SGE 406/D

RADIO COMMUNICATIONS GUIDE

MOTOROLA

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Introduction 1

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INTRODUCTION

The demand for standard semiconductor devices increased considerably in the last 5 - 6 years with introductions of VHF mobile radio and cordless telephones.

New developments in UHF (450 - 900 MHZ) cellular radio and cordless telephones has generated a need for highly specialised devices and R.F. modules.

The fast-growing European market, notably based on TACS, NMT, CNET and CEPT standards calls for a dedicated device selector guide.

This brochure presents (under a single cover) a compilation of summarised information found on the front pages of data sheets related to Motorola Radio Communication products and devices.

Detailed technical data is available in data books, data sheets and specific application notes. Copies of data sheets and application notes can be obtained from Motorola Sales Office or distributors listed on the back cover.

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Alpha/Numeric List of Products

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ALPHA/NUMERIC LIST OF PRODUCTS

ALPHA/NUMERIC LIST OF PRODUCTS (continued)

ALPHA/NUMERIC LIST OF PRODUCTS (continued)

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List of Products by Function

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LIST OF PRODUCTS BY FUNCTION

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Selector Guides for RF Modules and Discretes

RF Selector Guide

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SELECTOR GUIDES FOR RF MODULES AND DISCRETES

* LAND MOBILE POWER HYBRID AMPLIFIERS
* GENERAL PURPOSE WIDEBAND HYBRID AMPLIFIERS
* 407 – 512 MHZ UHF FM POWER TRANSISTORS
* 806 – 960 MHZ FM POWER TRANSISTORS
* 136 – 225 MHZ FM POWER TRANSISTORS

* 407 – 512 MHZ UHF RM POWER TRANSISTORS
* 806 – 960 MHZ UHF FM POWER TRANSISTORS
* 136 – 225 MHZ UHF FM POWER TRANSISTORS

* RF LOW NOISE AMPLIFIER TRANSISTORS
* FIELD EFFECT TRANSISTORS

* TUNING DIODES
* HYPER ABRUPT DIODES UHF/VHF
* SCHOTTKY DIODES
* PIN DIODES

LAND MOBILE POWER HYBRID AMPLIFIERS							
	Device Type	P Out Watts	P In Watts	Freq. MHZ	Power Gain dB Min	V CC Volts	Package
A	MHW709	7.5	0.1	400-512	18.8	12.5	700-03
A	MHW710	13	0.15	400-512	19.4	12.5	700-03
B	MHW720	20	0.15	400-470	21	12.5	700-03
B	MHW720A+	20	0.15	400-470	21	12.5	700-03
C	MHW802	2.2	0.05	825-915	20.4	9.5	784-01
D	MHW808	7.5	0.25	806-950	14.8	12.5	297A-05
D	MHW808A	7.5	0.03	806-950	24	12.5	301C-01
E	MHW812	12	0.5	890-915	13.8	12.5	297A-06
D	MHW820	20	0.25	806-950	19	12.5	301B-02

A: Available for 400-440 MHZ (−1); 440-470 MHZ (−2); 470-512 MHZ (−3)
B: Available for 400-440 MHZ (−1); 440-470 MHZ (−2)
C: Available for 825-845 MHZ (−1); 890-915 MHZ (−2)
D: Available for 806-870 MHZ (−1); 806-890 MHZ (−2); 870-950 MHZ (−3)
E: Available for 890-915 MHZ (−3)
\+ Designed for Wide Range P Out Level Control

GENERAL PURPOSE WIDEBAND HYBRID AMPLIFIERS — 50 OHMS TO-39 PACKAGE					
Device Type	Frequency Range	Gain dB Min/Typ	VCC Volts	Output Level 1 dB Compression DBM Typ	Noise Fig @250 MW D
MWA110	0.1-400	13/14	2.9	−2.5	4
MWA120	0.1-400	13/14	5	8.2	5.5
MWA130	0.1-400	13/14	5.5	18	7
MWA210	0.1-500	9/10	1.75	1.5	6
MWA220	0.1-600	9/10	3.2	10.5	6.5
MWA230	0.1-600	9/10	4.4	18.5	7.5
MWA310	0.1-1000	7/8	1.6	3.5	6.5
MWA320	0.1-1000	7/8	2.9	11.5	6.7
MWA330	0.1-1000	−/6.2	4	15.2	9

407–512 MHZ UHF FM POWER TRANSISTORS					
Device Type	P Out Watts	P In Watts	Power Gain dB Min	V CC Volts	Package
MRF629	2	0.32	8	12.5	TO-39
MRF630	3	0.33	9.5	12.5	TO-39
2N5944	2	0.25	9	12.5	244-04
2N5945	4	0.64	8	12.5	244-04
2N5946	10	2.5	6	12.5	244-04
MRF641	15	3.75	7.8	12.5	316-01
MRF644	25	5.9	6.2	12.5	316-01
MRF646	40	13.3	4.8	12.5	316-01
MRF648	60	22	4.4	12.5	316-01

806–960 MHZ FM POWER TRANSISTORS					
Device Type	P Out Watts	P In Watts	Power Gain dB Min	V CC Volts	Package
MRF837	1.75	0.125	8	12.5	MACRO-X
MRF557	1.5	0.25	8	12.5	317D-01
MRF839	3	0.5	8	12.5	305-01
MRF841	5	0.7	8.5	12.5	244-04
MRF840	10	2.5	6	12.6	319-04
MRF843	15	3	7	12.5	244-04
MRF842	20	5	6	12.5	319-04
MRF844	30	9	5.2	12.5	319-04
MRF846	40	15	4.3	12.5	319-04
MRF848	60	25	4	12.5	333A
MRF890	2	0.25	9	24	305-01
MRF891	5	0.62	9	24	319-04
MRF892	14	2	8.5	24	319-04
MRF894	30	6	7	24	319-04
MRF898	60	12	6.3	24	333A

136–225 MHZ FM POWER TRANSISTORS					
Device Type	P Out Watts	P In Watts	Power Gain dB Min	V CC Volts	Package
MRF2678	15	1	12	12.5	244-04
MRF1946	30	3	10	12.5	211-07

LOW NOISE AMPLIFIER TRANSISTORS

Device	Package	B . W Typ		Noise Figure (Max)			Gain		Max Ratings	
		FT GHZ	@ Ic mA	NF dB	@ f MHZ	IC mA	db Min	@ f MHZ	V(BR)CEO	Ic(mA)
MRF571	MACRO.X	8.0	50	2.0	1000	5.0	10.0	1000	10	70
MMBR571	SOT23	8.0	50	2.6	1000	10.0	10.5	1000	10	80
MRF2369	MACRO.X	6.0	50	2.0	1000	5.0	10.0	1000	15	70
MRF580	MACRO.X	5.0	75	2.0*	500	50.0	11.0	500	18	200
MRF581	MACRO.X	5.0	75	2.0*	500	50.0	13.0	500	18	200
BFQ19	SOT89	5.0	50	3.3	500	50.0			15	75
BFR91	MACRO.X	5.0	30	1.9*	500	2.0	16.0*	500	12	40
BFR93	SOT23	5.0	30	1.9*	500	2.0	–	–	15	35
MRF911	MACRO.X	5.0	30	2.5	1000	5.0	12.5*	1000	12	40
MMBR911	SOT23	5.0	30	2.5	1000	5.0				
MMBR930	SOT23	5.0	30	2.5*	1000	2.0	8.0*	500	12	35
BFR90	MACRO.X	5.0	14	2.4*	500	2.0	18.0*	500	15	30
BFR92	SOT23	5.0	14	2.4*	500	2.0	–	–	15	25
MRF901	MACRO.X	4.5	15	2.0	1000	5.0	10.0	1000	15	30
MMBR901	SOT23	4.5	15	1.9*	1000	5.0	16.0*	1000	15	30
MMBR920	SOT23	4.5	14	3.0*	1000	2.0	10.0*	1000	15	35
BFR96	MACRO.X	4.5	50	2.0*	500	10	12.0	500	15	100
BFQ18A	SOT89	4.0	50	–	–	–	–	–	15	150
MRF559	MACRO.X	3.0	100	–	–	–	13.0	512	18	150
MRF931	MACRO.X	3.0	1.0	3.8*	500	0.25	16.0*	500	5	5
MMBR931	SOT23	3.0	1.0	3.8*	500	0.25	10.0*	1000	5	5
MXR5943	SOT89	2.0	100	–	–	–	–	–	30	400
BFS17	SOT23	1.5	25	–	–	–	–	–	15	25
MMBR2060	SOT23	1.5	25	3.5	450	1.5	12.5	450	14	50
BFQ17	SOT89	1.2	150	–	–	–	–	–	25	300
MMBR5031	SOT23	1.0	5	2.5	450	1.0	14.0	450	10	20

* Typ

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FIELD EFFECT TRANSISTORS

Device	Package	Re	YFs	Noise Figure (Max)		I_{DSS} @ V_{DSS}=15V		Max Ratings	
		mm ho @ Min	f (MHZ)	dB Max	@ f (MHZ)	Min	Max	V(BR)GSS	I_B Max (mA)
2N5484	TO92	2.5	100	3.0	100	1.0	5.0	25	30
MMBF5484	SOT23	2.5	100	3.0	100	1.0	5.0	25	30
2N5486	TO92	3.5	400	3.5	400	8.0	20.0	25	30
MMBF5486	SOT23	3.5	400	3.5	400	8.0	20.0	25	30
MMBF4416	SOT23	4.0	400	4.0	400	5.0	15.0	30	20
U310	TO52	10	1kHZ	3.0*	450	24†	60†	25	100
MMBFU310	SOT23	10	1kHZ	3.0*	450	24†	60†	25	100
3N204	TO72	10	1kHZ	5.0	450	6.0	30	30	50

* Typ
† Measured @ V_{DS} = 10V

TUNING DIODES

Device*	Package	Nominal CAP ± 10% (pF) @ V_R=4V F=1 MHZ	CAP Ratio Min C2/C20	Q Typ @ 4V/50 MHZ	Max Rating V(BR) R
MMBV2097	SOT23	1.0	2.0	400	30V
MMBV2098	SOT23	2.2	2.0	400	30V
MMBV2101	SOT23	6.8	2.5	400	30V
MMBV2102	SOT23	8.2	2.5	350	30V
MMBV2103	SOT23	10	2.5	350	30V
MMBV2104	SOT23	12	2.5	350	30V
MMBV2105	SOT23	15	2.5	350	30V
MMBV2106	SOT23	18	2.5	300	30V
MMBV2107	SOT23	22	2.5	300	30V
MMBV2108	SOT23	27	2.5	250	30V
MMBV2109	SOT23	33	2.5	250	30V

*These Diodes exist also in TO92 (2 leads) Package

HYPER ABRUPT DIODES UHF/VHF

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Device	Package	Capacitance Min	Capacitance Max	(pF) @ VR(V)	Cap Ratio Min C3/C25	Q Typ @ 3V/50 MHZ	Max Rating V(BR)R
MMBV105G	SOT23	1.8	2.8	25	4	350	30V
MMBV3102	SOT23	20	25	3	4.5	300	30V
MMBV109	SOT23	26	32	3	5	250	30V
MV209	TO92	26	32	3	5	250	30V

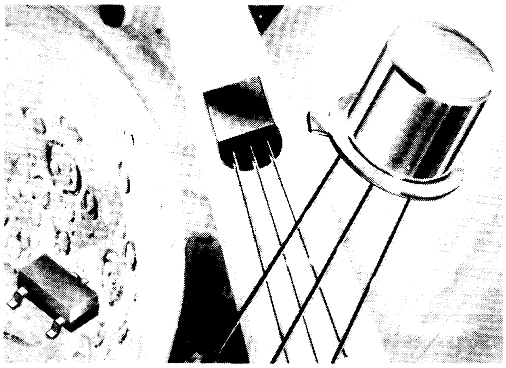
SCHOTTKY DIODES

Device	Package	Capacitance (pF) pF Max	@ V_R(Volts)	V_F Max (Volts) @ IF = 10 mA	Max Rating V(BR)R
MBD101	TO92	1	0	0.6	4V
MMBD101	SOT23	1	0	0.6	4V
MMBD352	SOT23	1	0	0.6	4V
MBD301	TO92	1.5	15	0.6	30V
MMBD301	SOT23	1.5	15	0.6	30V
MBD701	TO92	1	20	1.2	70V
MMBD701	SOT23	1	20	1.2	70V

PIN DIODES

Device	Package	Capacitance pF (Max)	@ V_R (Volts)	Resistance Ohms Max @ I_F=10 mA/100 MHZ	Max Rating V(BR)R
MPN3404	TO92	2	20	0.85	20
MMBV3401	SOT23	1	20	0.70	35
MMBV3700	SOT23	1	15	0.40	200

Package Outline Dimensions



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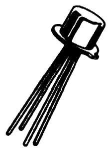
The following pages contain information on the various packages referenced on the individual data sheets. Information includes: a picture of the package, dimensions in both millimeters and inches, the various pinout configurations (styles), a cross reference for Case numbers, "old" JEDEC "TO" numbers, and the new JEDEC "TO" designation.

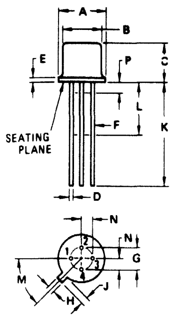
An information on Tape and Reel packaging capabilities is also given.

Package Outline Dimensions

Dimensions are in inches unless otherwise noted.

CASE 20-03 TO-72 (TO-206AF)

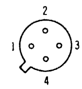




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20 STYLES



STYLE 1
PIN 1. SOURCE
2. DRAIN
3. GATE
4. CASE LEAD

STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

STYLE 3
PIN 1. DRAIN
2. SOURCE
3. GATE
4. CASE LEAD

STYLE 4
PIN 1. SOURCE
2. GATE
3. DRAIN
4. GATE 2 - SUBSTRATE AND CASE

STYLE 5
PIN 1. SOURCE
2. GATE 1
3. DRAIN
4. CASE

STYLE 6
PIN 1. DRAIN
2. SOURCE AND SUBSTRATE
3. GATE
4. SOURCE AND SUBSTRATE

STYLE 7
PIN 1. DRAIN
2. SOURCE
3. GATE
4. CASE AND SUBSTRATE

STYLE 8
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR
4. EMITTER 1 BASE 2

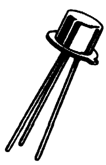
STYLE 9
PIN 1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE, SUBSTRATE AND CASE

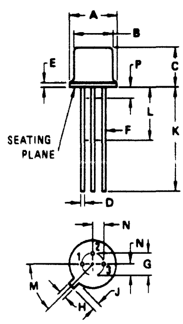
STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

STYLE 11
PIN 1. EMITTER
2. CATHODE
3. COLLECTOR
4. ANODE

NOTE:
1. ALL RULES AND NOTES WITH TO-72 OUTLINE SHALL APPLY

CASE 22-03 TO-18 (TO-206AA)

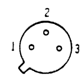




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

CASE 22 STYLES



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2
PIN 1. SOURCE,SUBSTRATE AND CASE
2. GATE
3. DRAIN

STYLE 3
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 4
PIN 1. SOURCE
2. DRAIN
3. GATE &CASE

STYLE 5
PIN 1. EMITTER
2. BASE 1
3. BASE 2

STYLE 6
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 7
PIN 1. ANODE
2. BASE
3. CATHODE

STYLE 8
PIN 1. GATE
2. ANODE 1
3. ANODE 2

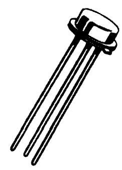
STYLE 9
PIN 1. ANODE 2
2. ANODE 1
3. GATE (CONNECTED TO CASE)

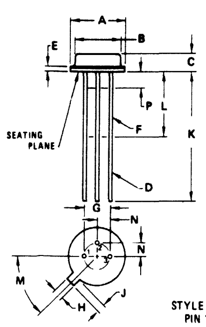
STYLE 10
PIN 1. BASE
2. EMITTER
3. BASE

STYLE 11
PIN 1. DRAIN
2. GATE
3. SOURCE, SUBSTRATE

STYLE 12:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

CASE 26-03 TO-46 (TO-206AB)



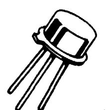


STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	1.65	2.16	0.065	0.085
D	0.406	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.305	0.483	0.012	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC dimensions and notes apply

CASE 27-02 TO-52 (TO-206AC)

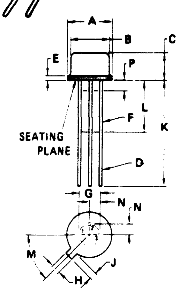


STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. DRAIN
2. SOURCE
3. GATE & CASE

STYLE 3:
PIN 1. EMITTER
2. BASE
3. BASE 2

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE & CASE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	2.92	3.81	0.115	0.150
D	–	0.533	–	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC dimensions and notes apply

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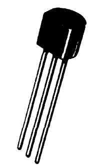
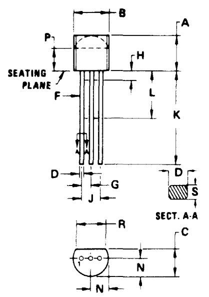
PACKAGE OUTLINE DIMENSIONS (continued)

CASE 29-02 TO-92 (TO-226AA)

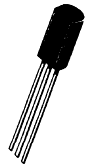


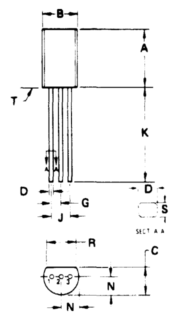


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.67	0.080	0.105
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-03 TO-226AE





NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS:
   | ⌖ | Ø 0.10 (0.004) Ⓜ | T | A Ⓜ | B Ⓜ |
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.37	7.87	0.290	0.310
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.46	0.61	0.018	0.024
G	1.27 BSC		0.050 BSC	
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
N	2.03	2.92	0.080	0.115
R	3.43	–	0.135	–
S	0.46	0.61	0.018	0.024

CASE 29 STYLES

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

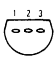
STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE



STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
1. MT 1
2. GATE
3. MT 2.

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

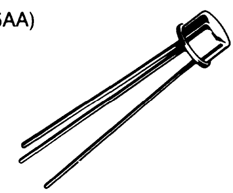
STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

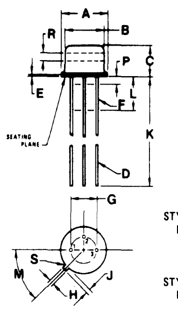
STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 31-03 TO-5 (TO-205AA)





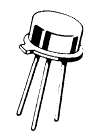
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

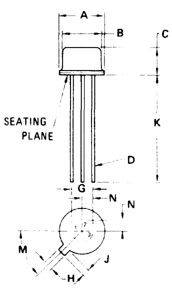
STYLE 2:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 3:
PIN 1. GATE
2. CATHODE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.711	0.864	0.028	0.034
J	0.734	1.14	0.029	0.045
K	38.10	44.45	1.500	1.750
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	——		——	
P	–	1.27	–	0.050
R	2.54	–	0.100	–
S	–	0.25	–	0.010

CASE 31A-01





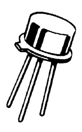
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

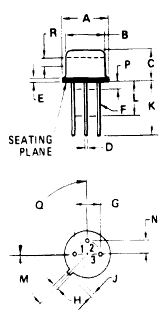
STYLE 2:
PIN 1. INPUT
2. OUTPUT
3. GROUND

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.57	0.150	0.180
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

NOTE:
1. LEADS WITHIN 0.36 mm (0.014) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

CASE 79-02 TO-39 (TO-205AD)



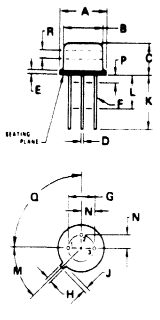


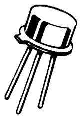
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

PACKAGE OUTLINE DIMENSIONS (continued)

CASE 79-03

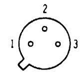




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.02	9.30	0.355	0.366
B	8.00	8.51	0.315	0.335
C	4.19	4.57	0.165	0.180
D	0.43	0.53	0.017	0.021
E	0.43	0.89	0.017	0.035
F	0.41	0.48	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.71	0.86	0.028	0.034
J	0.74	1.02	0.029	0.040
K	12.70	–	0.500	–
M	45° NOM		45° NOM	
N	2.54 TYP		0.100 TYP	
Q	90° NOM		90° NOM	

CASE 79 STYLES

PIN 1. INPUT
2. OUTPUT
3. GROUND



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 3
PIN 1. CATHODE
2. GATE
3. ANODE

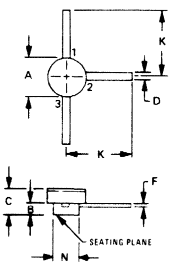
STYLE 4
PIN 1. MAIN TERM. 1
2. GATE
3. MAIN TERM. 2

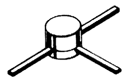
STYLE 5
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH TO-39 OUTLINE SHALL APPLY.

CASE 176-02

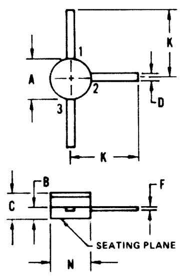


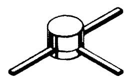


NOTE:
A Tolerance of .25 mm (.010) must be allowed at point leads protrude from package for glass run over.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.03	2.67	0.080	0.105
B	0.38	0.76	0.015	0.030
C	1.27	2.03	0.050	0.080
D	0.25	0.41	0.010	0.016
F	0.08	0.15	0.003	0.006
K	4.06	4.57	0.160	0.180
N	1.47	1.78	0.058	0.070

CASE 176B-01





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.03	2.67	0.080	0.105
B	0.38	0.76	0.015	0.030
C	1.27	2.03	0.050	0.080
D	0.25	0.41	0.010	0.016
F	0.08	0.015	0.003	0.006
K	4.06	4.57	0.160	0.180
N	2.03	2.67	0.080	0.105

CASE 176 STYLES

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 3:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 4:
PIN 1. ANODE 2
2. ANODE 1
3. CATHODE

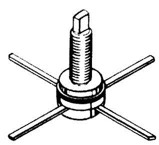
STYLE 5:
PIN 1. CATHODE
2. NOT CONNECTED
3. ANODE

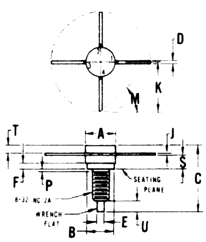
STYLE 6:
PIN 1. CATHODE
2. ANODE
3. ANODE

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NC
3. CATHODE

CASE 244A-01





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

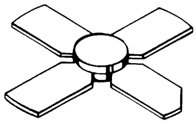
STYLE 2:
PIN 1. COMMON
2. OUTPUT
3. COMMON
4. INPUT

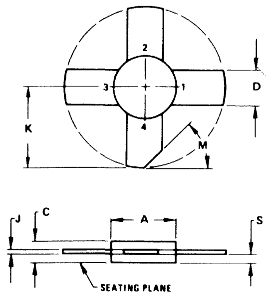
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.10	0.15	0.004	0.006
K	11.17	–	0.440	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

4

PACKAGE OUTLINE DIMENSIONS (continued)

CASE 249-05





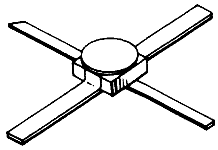
STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

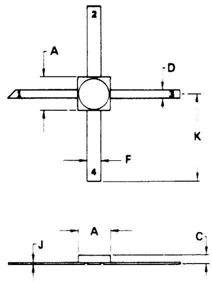
STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

SEATING PLANE = GROUND AND IS CONNECTED TO PIN 1 AND PIN 3.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
C	2.84	3.45	0.112	0.136
D	5.46	5.97	0.215	0.235
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
S	1.40	1.65	0.055	0.065

CASE 303-01





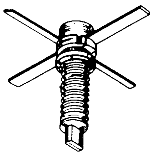
STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

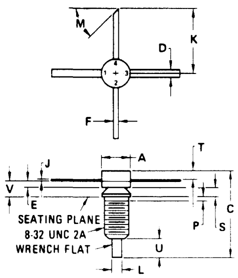
STYLE 2:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. BASE

NOTE:
1. DIMENSION K APPLIES TO ALL LEADS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.29	2.67	0.090	0.105
C	0.89	1.40	0.035	0.055
D	0.41	0.61	0.016	0.024
F	0.89	1.09	0.035	0.043
J	0.08	0.15	0.003	0.006
K	4.45	5.84	0.175	0.230

CASE 305-01

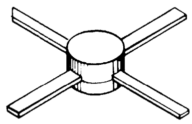


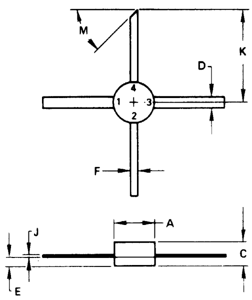


STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.08	5.59	0.200	0.220
C	13.97	16.26	0.550	0.640
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	1.40	1.65	0.055	0.065
T	1.40	1.78	0.055	0.070
U	2.79	3.81	0.110	0.150
V	2.41	2.92	0.095	0.115

CASE 305A-01

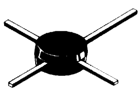


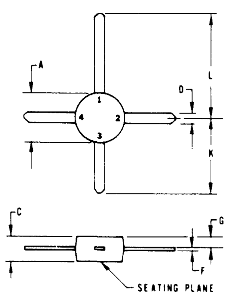


STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.08	5.59	0.200	0.220
C	2.41	3.30	0.095	0.130
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	

CASE 317-01



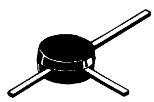


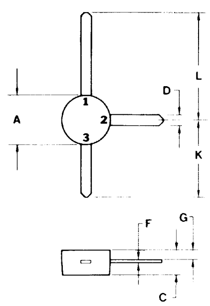
STYLE 1:
PIN 1. DRAIN
2. SOURCE
3. GATE 1
4. GATE 2

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

CASE 317A-01





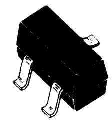
STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

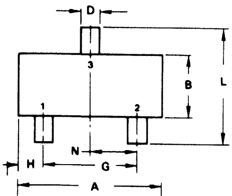
STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.94	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

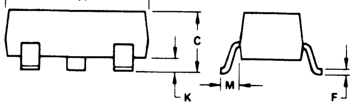
PACKAGE OUTLINE DIMENSIONS (continued)

CASE 318 TO-236AA

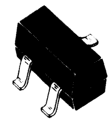


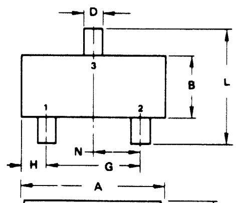


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.46	0.015	0.0177
F	0.085	0.13	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.020	0.0236
K	0.10	0.25	0.004	0.0098
L	2.10	2.50	0.083	0.0984
M	0.45	0.60	0.018	0.0236
N	0.89	1.02	0.035	0.0401

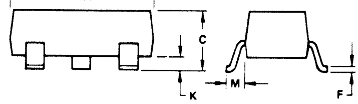


CASE 318 TO-236AB (Low Profile)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.04	0.035	0.0412
D	0.37	0.46	0.015	0.0177
F	0.085	0.13	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.020	0.0236
K	0.013	0.10	0.0005	0.0040
L	2.10	2.50	0.083	0.0984
M	0.45	0.60	0.018	0.0236
N	0.89	1.02	0.035	0.0401



CASE 318 STYLES

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE
ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

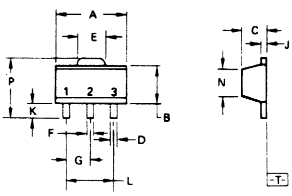
STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

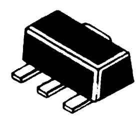
STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLES 1 THRU 5 ARE OBSOLETE.

NOTES
1. 318-02 MEETS ALL JEDEC DIMENSIONAL REQUIREMENTS FOR TO-236 AA.

CASE 345-01





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.40	4.60	0.174	0.181
B	2.29	2.60	0.091	0.102
C	1.40	1.60	0.056	0.062
D	0.36	0.48	0.015	0.018
E	1.62	1.80	0.064	0.070
F	0.44	0.53	0.018	0.020
G	1.50 BSC		0.059 BSC	
J	0.35	0.44	0.014	0.017
K	0.80	1.04	0.032	0.040
L	3.00 BSC		0.118 BSC	
N	2.04	2.28	0.081	0.089
P	3.94	4.25	0.156	0.167

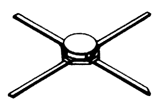
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

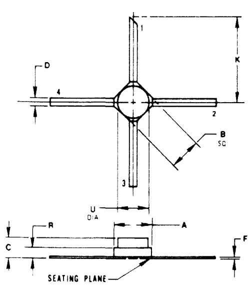
STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NO CONNECTION

STYLE 3:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 358-01



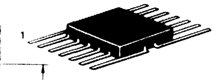


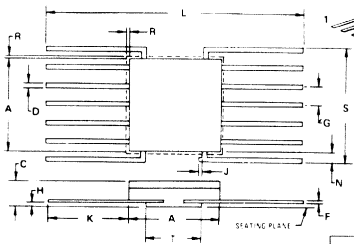
STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 2:
PIN 1. DRAIN
2. SOURCE
3. GATE 1
4. GATE 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.41	2.92	0.095	0.115
B	1.95	2.36	0.077	0.093
C	1.09	1.60	0.043	0.063
D	0.43	0.58	0.017	0.023
F	0.07	0.15	0.003	0.006
K	4.82	6.60	0.190	0.260
R	0.53	0.96	0.021	0.038
U	1.98	2.18	0.078	0.086

CASE 607-04 CERAMIC



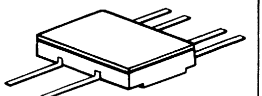


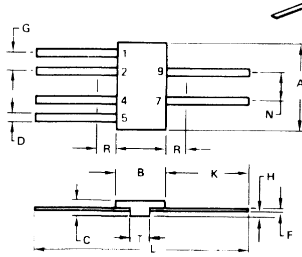
STYLE 1
BASE 2, 6, 9, 13
EMITTER 3, 5, 10, 12
COLLECTOR 1, 7, 8, 14
FOR COMPLEMENTARY QUADS
NPN PINS 1 THRU 3, 12 THRU 14
PNP PINS 5 THRU 7, 8 THRU 10
(REFER TO STYLE 1
FOR PIN IDENTIFICATION)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.99	0.240	0.275
C	0.76	2.03	0.030	0.070
D	0.25	0.48	0.010	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
J	–	0.38	–	0.015
K	6.35	–	0.250	–
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330
T	4.45	4.95	0.175	0.195

PACKAGE OUTLINE DIMENSIONS (continued)

CASE 610A-04 CERAMIC

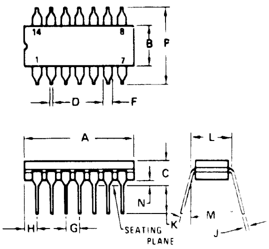


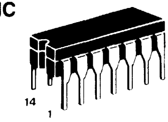


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	7.37	0.240	0.290
B	2.92	4.06	0.115	0.160
C	0.76	2.03	0.030	0.070
D	0.36	0.48	0.014	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
K	3.81	-	0.150	-
L	10.54	-	0.415	-
N	2.54 BSC		0.100 BSC	
R	-	1.27	-	0.050
T	1.65	2.03	0.065	0.080

STYLE 1
BASE 1, 5
EMITTER 2, 4
COLLECTOR 9, 7
FOR COMPLEMENTARY PAIRS
NPN PINS 1, 2, 9
PNP PINS 4, 5, 7
(REFER TO STYLE 1 FOR PIN IDENTIFICATION)

CASE 632-02 TO-116 CERAMIC

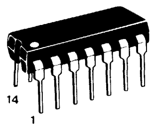


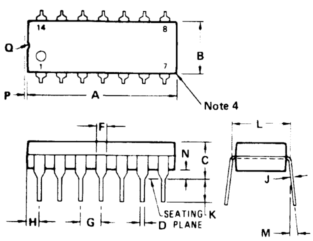


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	-	5.08	-	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	-	0.100	-
L	7.62 BSC		0.300 BSC	
M	-	15°	-	15°
N	0.51	0.76	0.020	0.030
P	-	8.25	-	0.325

STYLE 1
COLLECTOR 1, 7, 8, 14
BASE 2, 6, 9, 13
EMITTER 3, 5, 10, 12
COMPLEMENTARY PAIRS
TYPE 1 — NPN 1 THRU 3, 5 THRU 7; PNP 8 THRU 10, 12 THRU 14
TYPE 2 — NPN 1 THRU 3, 12 THRU 14; PNP 5 THRU 7, 8 THRU 10
(REFER TO STYLE 1 FOR PIN IDENTIFICATION)

CASE 646-05

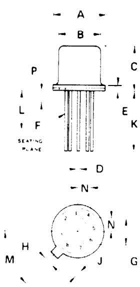


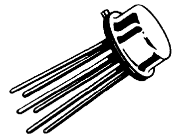


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

STYLE 1
BASE 2, 6, 9, 13
EMITTER 3, 5, 10, 12
COLLECTOR 1, 7, 8, 14
COMPLEMENTARY PAIRS
TYPE 1 — NPN 1 THRU 3, 5 THRU 7; PNP 8 THRU 10, 12 THRU 14
TYPE 2 — NPN 1 THRU 3, 12 THRU 14; PNP 5 THRU 7, 8 THRU 10
(REFER TO STYLE 1 FOR PIN IDENTIFICATION)

CASE 654-02

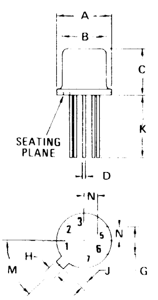


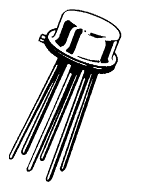


NOTES:
1. ALL RULES & NOTES ASSOCIATED WITH REFERENCED TO-78 (654-02) OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.53	0.016	0.021
E	–	1.02	–	0.040
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	2.54		0.100 BSC	
P	–	1.27	–	0.050

CASE 654-07





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.70	0.150	0.185
D	0.41	0.53	0.016	0.021
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70		0.500	-
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 654 STYLES

STYLE 1:
PIN 1. COLLECTOR — 5. EMITTER
2. BASE — 6. BASE
3. EMITTER — 7. COLLECTOR
4. OMITTED — 8. OMITTED

STYLE 2:
PIN 1. COLLECTOR — 5. SOURCE
2. BASE — 6. DRAIN
3. EMITTER — 7. GATE
4. OMITTED — 8. OMITTED

STYLE 3:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. OMITTED
5. ANODE
6. NO CONNECTION
7. CATHODE
8. OMITTED

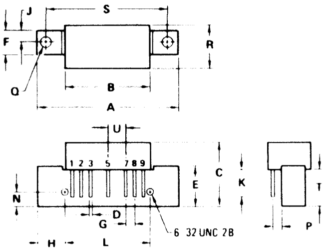
STYLE 4:
PIN 1. GATE — 5. DRAIN
2. SOURCE — 6. SOURCE
3. DRAIN — 7. GATE
4. OMITTED — 8. OMITTED

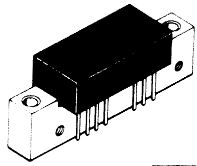
STYLE 5:
SIDE 1 (NPN) — SIDE 2 (PNP)
PIN 1. COLLECTOR — 5. EMITTER
2. BASE — 6. BASE
3. EMITTER — 7. COLLECTOR
4. OMITTED — 8. OMITTED

STYLE 6:
PIN 1. SOURCE — 5. SOURCE
2. DRAIN — 6. DRAIN
3. GATE — 7. GATE
4. OMITTED — 8. OMITTED

PACKAGE OUTLINE DIMENSIONS (continued)

CASE 714-02





FIRST STAGE PIN 1, RF IN
4, RF OUT

SECOND STAGE PIN 6, RF IN
9, RF OUT

Vdc PIN 5

DC AND RF GROUND PINS 2, 3, 7, 8

NOTE
1 MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		45.08		1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.13	0.300	0.320
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	6.86	7.37	0.270	0.290
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R		15.11		0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

4

4

Front Page of Data Sheets of Integrated Circuits

5

MOTOROLA

MC12000

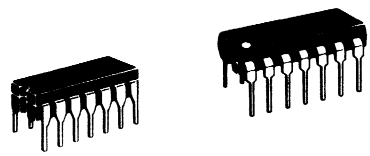
DIGITAL MIXER/TRANSLATOR
(D Flip-Flop w/Translator)

The MC12000 is intended for use as a digital mixer in phase-locked loop frequency synthesizers and other applications where a MECL "D" flip-flop with translators is required. Toggle frequency is typically 250 MHz. TTL to MECL and MECL to TTL translators are provided to facilitate interfacing with MECL or TTL circuits.

The MC12000 is designed to operate from a single power supply of either +5.0 Vdc or −5.2 Vdc.

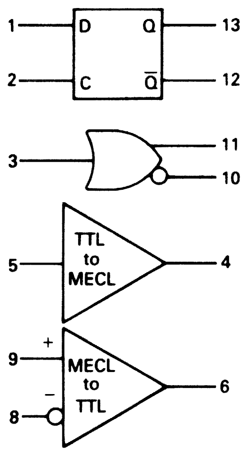
DIGITAL MIXER/TRANSLATOR

P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632

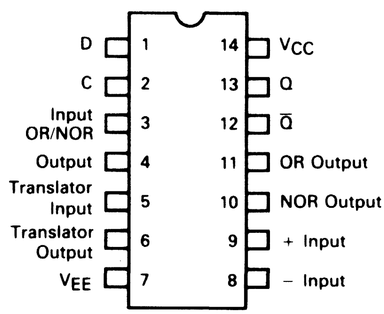
LOGIC DIAGRAM



D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

V_{CC} = Pin 14
V_{EE} = Pin 7

PIN ASSIGNMENT



MOTOROLA

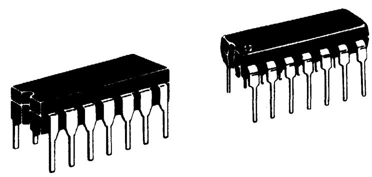
MC12002/ MC12502

ANALOG MIXER

ANALOG MIXER

The MC12002/MC12502 is a double balanced analog mixer, including an input amplifier feeding the mixer carrier port and a temperature compensated bias regulator. The input circuits for both the amplifier and mixer are differential amplifier circuits. The on-chip regulator provides all of the required biasing.

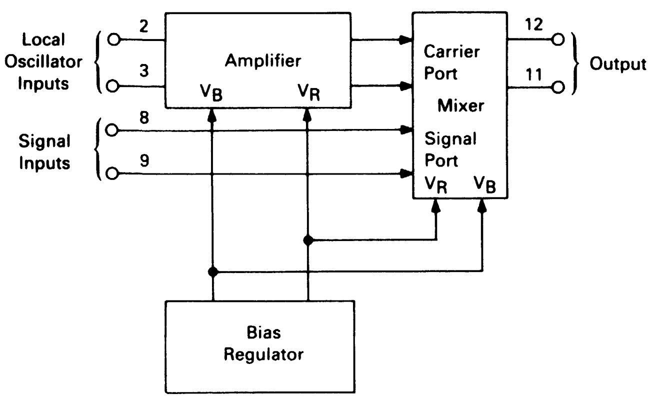
This circuit is designed for use as a balanced mixer in high-frequency wide-band circuits. Other typical applications include suppressed carrier and amplitude modulation, synchronous AM detection, FM detection, phase detection, and frequency doubling, at frequencies up to UHF.



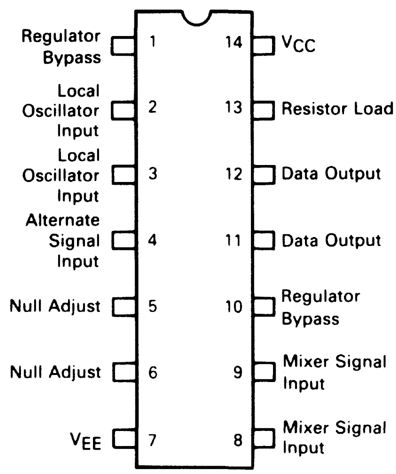
P SUFFIX
PLASTIC PACKAGE
CASE 646

L SUFFIX
CERAMIC PACKAGE
CASE 632-02

LOGIC DIAGRAM



PIN ASSIGNMENT



MOTOROLA

MC12009 MC12509
MC12011 MC12511
MC12013 MC12513

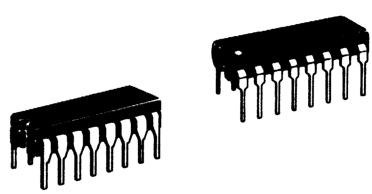
TWO-MODULUS PRESCALER

These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-TTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source. Details of operation are on the MC12012 data sheet.

- 600 MHz (Typ) Toggle Frequency
- MC12009 (÷5/6), MC12011 (÷8/9), MC12013 (÷10/11)
- MECL to TTL Translator on Chip
- MECL and TTL Enable Inputs
- +5.0 or −5.2 V Operation*
- Buffered Clock Input — Series Input RC Typ, 20 Ohms and 4 pF
- V_{BB} Reference Voltage
- 310 Milliwatts (Typ)

*When using +5.0 V supply, apply +5.0 V to pin 1 (V_{CCO}), pin 6 (TTL V_{CC}), pin 16 (V_{CC}), and ground pin 8 (V_{EE}). When using −5.2 V supply, ground pin 1 (V_{CCO}), pin 6 (TTL V_{CC}), and pin 16 (V_{CC}) and apply −5.2 V to pin 8 (V_{EE}). If the translator is not required, pin 6 may be left open to conserve dc power drain.

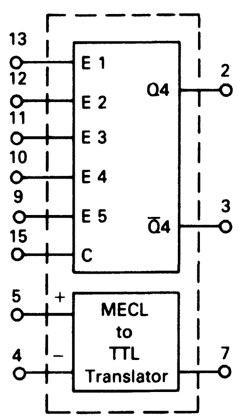
TWO-MODULUS PRESCALER



P SUFFIX
PLASTIC PACKAGE
CASE 648

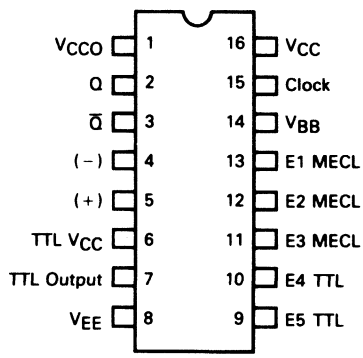
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CCO} = pin 1
V_{CC} = pin 16
V_{EE} = pin 8

PIN ASSIGNMENT



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ADI-534R1

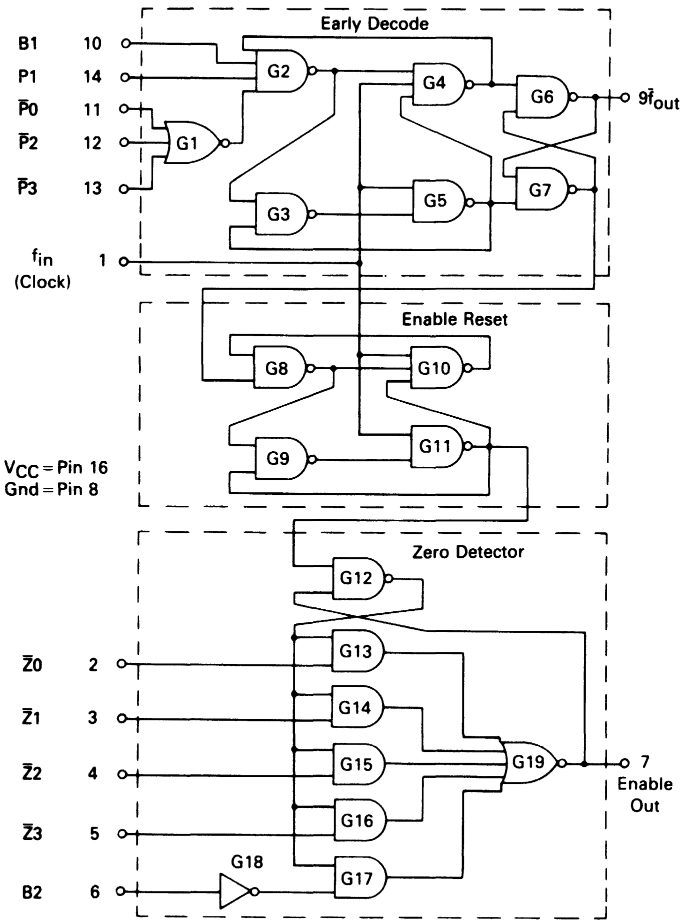
MOTOROLA

MC12014/ MC12514

COUNTER CONTROL LOGIC

The MC12014 monolithic counter control logic unit is designed for use with the MC12013 Two-Modulus Prescaler and the MC4016 Programmable Counter to accomplish direct high-frequency programming. The MC12014 consists of a zero detector which controls the modulus of the MC12013, and an early decode function which controls the MC4016. The early decode feature also increases the useful frequency range of the MC4016 from 8.0 MHz to 25 MHz.

LOGIC DIAGRAM



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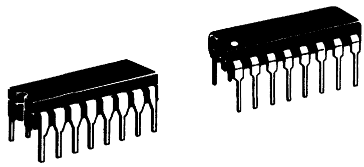
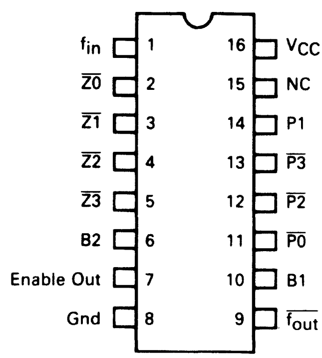
COUNTER CONTROL LOGIC

P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



DS 9236 (Issue B)

MOTOROLA

MC12015
MC12016
MC12017

Advance Information

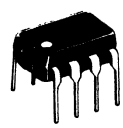
LOW-POWER TWO-MODULUS PRESCALER

The MC12015, MC12016 and MC12017 are two-modulus prescalers which will divide by 32 and 33, 40 and 41, and 64 and 65 respectively. An internal regulator is provided to allow these devices to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 225 MHz Toggle Frequency
- Low-Power—7.5 mA Max at 6.8 V
- Control Input and Output are Compatible with Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V

MECL PLL COMPONENTS

LOW-POWER
TWO - MODULUS
PRESCALER



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

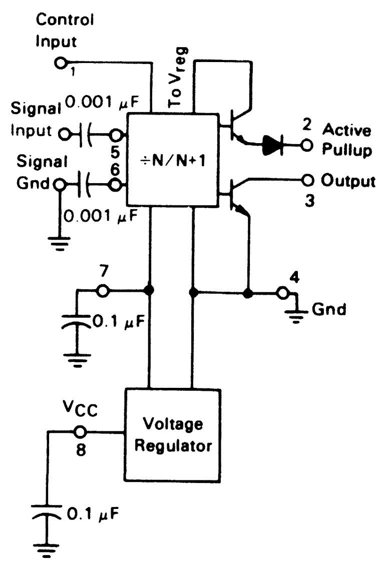
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V, T_A = -40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}	225	—	—	MHz
	f_{min}	—	—	35	MHz
Supply Current	I_{CC}	—	6.0	7.8	mA
Control Input High (÷32, 40 or 64)		2.0	—	—	V
Control Input Low (÷33, 41 or 65)		—	—	0.8	V
Output Voltage High* (I_{source} = 50 μA)	V_{OH}	2.5	—	—	V
Output Voltage Low* (I_{sink} = 2 mA)	V_{OL}	—	—	0.5	V
Input Voltage Sensitivity 35 MHz	V_{in}	400	—	800	
50-255 MHz		200	—	800	mVPP
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out} -70	ns

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

*Pin 2 connected to Pin 3

PRESCALER BLOCK DIAGRAM



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ADI-626R2

MOTOROLA

MC12018

Product Preview

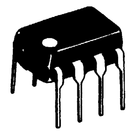
MECL PLL COMPONENTS

÷128/129
LOW-POWER
TWO-MODULUS
PRESCALER

÷128/129 520 MHz LOW-POWER TWO-MODULUS PRESCALER

The MC12018 is a two-modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 520 MHz Toggle Frequency
- Low-Power — 7.0 mA Typical
- Control Input Is Compatible with Standard CMOS and TTL
- Supply Voltage 4.5 V to 9.5 V
- The Specifications of This Product Preview Are Design Goals Only



P SUFFIX
PLASTIC PACKAGE
CASE 626

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MAXIMUM RATINGS

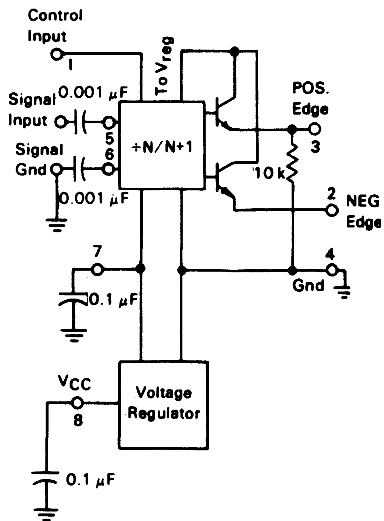
Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V T_A = -40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max}	520	—	—	MHz
Supply Current (Pin 8)	I_{CC}	—	7.0	—	mA
Control Input High (÷ 128)	V_{IH}	2.0	—	—	V
Control Input Low (÷ 129)	V_{IL}	—	—	0.8	V
Differential Output Voltage (I_{sink} = 200 µA)	V_{out}	0.8	1.0	—	V
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out}-35	ns
Input Voltage Sensitivity	V_{in}	200	—	800	mVpp

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform

PRESCALER BLOCK DIAGRAM



NP 149R

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MOTOROLA

MC12019

Advance Information

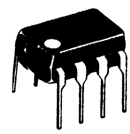
LOW-POWER TWO-MODULUS PRESCALER

The MC12019 is a divide by 20 and 21 two-modulus prescaler. It will divide by 20 when the modulus control input is high and by 21 when the modulus control input is low.

- 225 MHz Toggle Frequency
- Low-Power—7.5 mA Max at 5.5 V
- Control Input Compatible with Standard Motorola CMOS Synthesizers
- Emitter Follower Outputs

MECL PLL COMPONENTS

LOW-POWER TWO - MODULUS PRESCALER
÷20/21



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

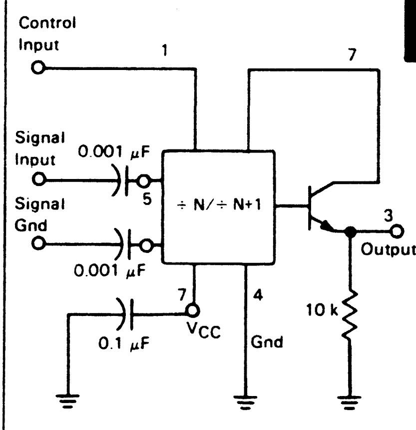
Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 7	V_{CC}	8.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = -40° to +85° C)

Characteristic	Symbol	-40°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
Toggle Frequency (Sine wave input)	f_{max} f_{min}	225 —	— 35	225 —	— 35	225 —	— 35	MHz MHz
Supply Current	I_{CC}	—	7.5	—	7.5	—	7.5	mA
Control Input High (÷20)		2.0	—	2.0	—	2.0	—	V
Control Input Low (÷20)		—	0.8	—	0.8	—	0.8	V
Output Voltage Swing	V_{out}	—	600	—	600	—	600	mV_{pp}
Input Voltage Sensitivity 35 MHz 50-255 MHz	V_{in}	 400 200	 800 800	 400 200	 800 800	 400 200	 800 800	
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	t_{out}-70	—	t_{out}-70	—	t_{out}-70	ns

Notes:
1. t_{PLL} = the time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

PRESCALER BLOCK DIAGRAM



ADI-710R1

MC12022

Product Preview

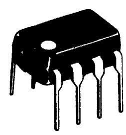
÷128/129 1.0 GHz LOW-POWER TWO-MODULUS PRESCALER

The MC12022 is a two-modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 1.0 GHz Toggle Frequency
- Low-Power 14 mA Typical
- Control Input Is Compatible with Standard CMOS and TTL
- Supply Voltage 4.5 V to 9.5 V
- Propagation Delay 25 ns Typical
- The Specifications of This Product Preview Are Design Goals Only

MECL PLL COMPONENTS

÷128/129 LOW-POWER TWO-MODULUS PRESCALER



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

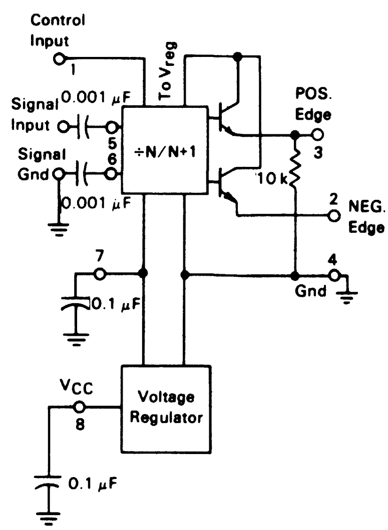
Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V, T_A = -40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max}	1.0	—	—	GHz
Supply Current (Pin 8)	I_{CC}	—	14	—	mA
Control Input High (÷ 128)	V_{IH}	2.0	—	—	V
Control Input Low (÷ 129)	V_{IL}	—	—	0.8	V
Differential Output Voltage (I_{sink} = 200 μA)	V_{out}	0.8	1.0	—	V
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out} -50	ns
Input Voltage Sensitivity	V_{in}	200	—	800	mVpp

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

PRESCALER BLOCK DIAGRAM



NP 150R1

MOTOROLA

MC12023

Advance Information

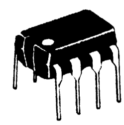
MECL PLL COMPONENTS

LOW-POWER PRESCALER ÷ 64

÷ 64, 225 MHz, LOW-POWER PRESCALER

The MC12023 is a new member of Motorola's PLL family. The MC12023 is a prescaler which will divide by 64. This device may be operated over a wide range of supply voltages (3.2 to 5.5 V). Because of this range of supply voltages the MC12023 is very suitable for hand-held, battery-operated devices.

- 225 MHz Toggle Frequency
- Low-Power — 4.0 mA Maximum at 5.5 V
- Operating Supply Voltage — 3.2 V to 5.5 V
- Connecting Pins 2 and 3 Allows Driving One TTL Load



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	0 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.2 to 5.5 V, T_A = 0°C to +70°C)

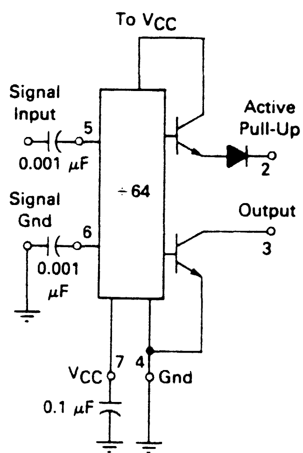
Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency	f_{max}	225	—	—	MHz
(Sine wave input)	f_{min}	—	—	20	MHz
Supply Current	I_{CC}	—	3.5**	4.0	mA
Output Voltage High* (I_{source} = 50 μA, V_{CC} = 3.2 V)	V_{OH}	1.2	1.4	—	V
Output Voltage High* (I_{source} = 50 μA, V_{CC} = 5.0 V)	V_{OH}	3.5	—	—	V
Output Voltage Low* (I_{sink} = 2.0 mA)	V_{OL}	—	—	0.5	V
Input Voltage Sensitivity 35 MHz	V_{in}	400	—	800	mVpp
Input Voltage Sensitivity 50–225 MHz	V_{in}	200	—	800	mVpp
AC Input Resistance	R_{in}	—	TBA	—	kΩ
Input Capacitance	C_{in}	—	TBA	—	pF

*Pin 2 connected to Pin 3
**V_{CC} = 4.5 V

TBA — To Be Announced.

his document contains information on a new product. Specifications and information herein re subject to change without notice.

PRESCALER BLOCK DIAGRAM



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MOTOROLA

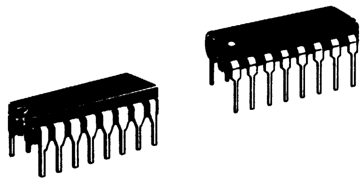
MC12040/
MC12540

PHASE-FREQUENCY DETECTOR

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

Operating Frequency = 80 MHz typical

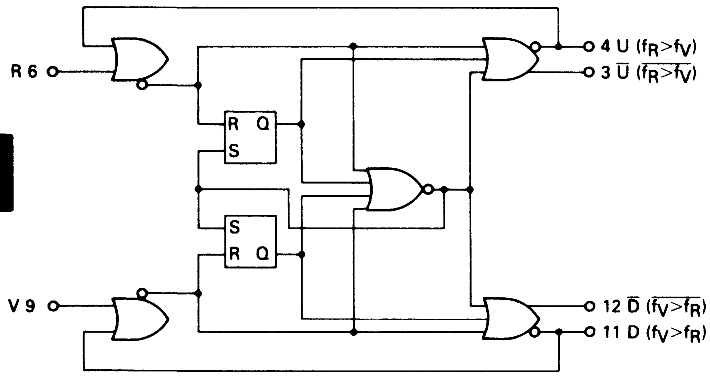
PHASE-FREQUENCY DETECTOR



P SUFFIX
PLASTIC PACKAGE
CASE 646

L SUFFIX
CERAMIC PACKAGE
CASE 632-02

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

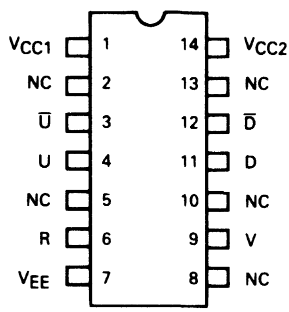
TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

INPUT		OUTPUT			
R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	0

X = Don't Care

PIN ASSIGNMENT



NC — No Connection

MOTOROLA

MC12061 • MC12561

CRYSTAL OSCILLATOR

CRYSTAL OSCILLATOR

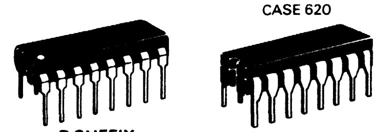
The MC12061 and MC120561 are designed for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and TTL outputs.

Frequency Range = 2.0 MHz to 20 MHz

Single Supply Operation: + 5.0 Vdc or −5.2 Vdc

Three Outputs Available:

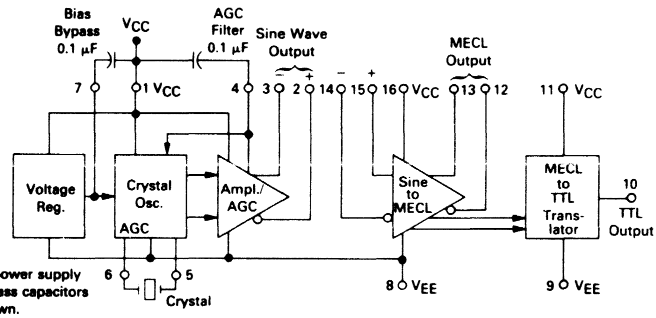
1. Complementary Sine Wave (600 mVp-p typ)
2. Complementary MECL
3. Single Ended TTL



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM



Note: 0.1 µF power supply pin bypass capacitors not shown.

TYPICAL CIRCUIT CONFIGURATIONS Note: 0.1 µF power supply pin bypass capacitors not shown.

FIGURE 2 — SINE WAVE OUTPUT

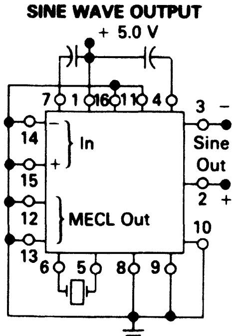


FIGURE 3 — MTTL OUTPUT

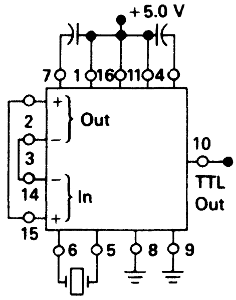


FIGURE 4 — MECL OUTPUT (+5.0 V Supply)

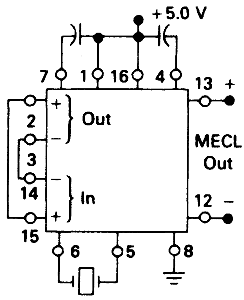
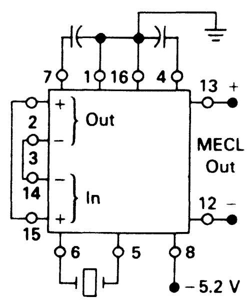


FIGURE 5 — MECL OUTPUT (−5.2 V Supply)



CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	MC12061/12561
Mode of Operation	Fundamental Series Resonance
Frequency Range	2.0 MHz - 20 MHz
Series Resistance, R1	Minimum at Fundamental
Maximum Effective Resistance, $R_{E(max)}$	155 ohms

MOTOROLA

MC12071

HIGH-SPEED PRESCALER

The MC12071 is a high-speed prescaler designed for use in communications and instrumentation systems. In the UHF mode, it performs division by 256, and divides by 64 in the VHF mode.

A bandswitch mode control line selects the mode of operation between the UHF and VHF input pins.

UHF operation is selected by applying a high-level (logical 1) to the bandswitch input. A low-level (logical 0) is applied to the bandswitch input to obtain the VHF mode. An internal amplifier/multiplexer is used to isolate both inputs, amplify the input signal, and improve sensitivity.

Inputs are designed for ac-coupled sine wave signals, but can be dc-coupled if proper bias levels are maintained. Normally used single-ended, the inputs can also be operated with complementary input signals if required.

Circuit outputs are complementary emitter-follower type which can drive a 33-pF or equivalent load. Maintaining a balanced load and controlling rise and fall times will reduce harmonic outputs.

- Broadband Operation
- High Sensitivity
- Standard 5 Volt Power Supply
- VHF/UHF — Dual Mode Operation
- Complementary Emitter-Follower Outputs
- Independent VHF and UHF Input Pins

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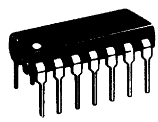
HIGH-SPEED PRESCALER

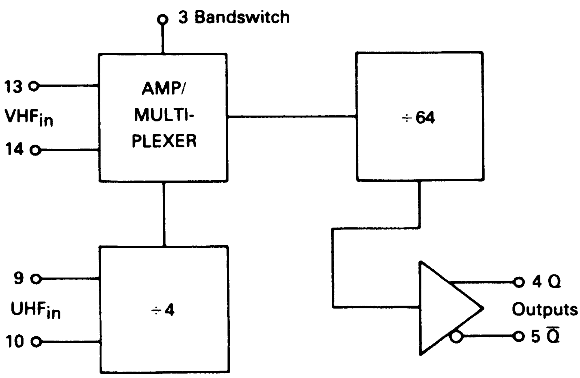


P SUFFIX
PLASTIC PACKAGE
CASE 646

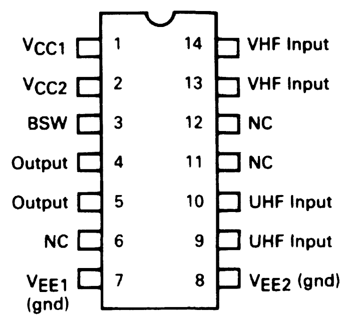
TYPICAL APPLICATIONS

- CATV Converters
- Digital frequency synthesizers for:
  - VHF/UHF receivers
  - Instrumentation
  - Satellite communications
- High-frequency divider for:
  - Frequency counters (UHF)
  - Timers (UHF)
  - High-Speed computers
  - SHF, second IF local-oscillator injection
  - Frequency standards
  - PCM communications
  - Radar ranging systems
  - Satellite communications
- High-frequency up-converters

LOGIC DIAGRAM



PIN ASSIGNMENT



NC — No Connection

MOTOROLA

MC12073

Product Preview

÷64 LOW-POWER PRESCALER

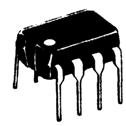
The MC12073 is a new member of Motorola's PLL family. It is a high-speed, low-power prescaler which divides by 64. The MC12073 can be used in all frequency synthesis applications. Typical applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included in the MC12073. This preamplifier isolates the differential inputs and provides gain for the input signal. The MC12073 is pin compatible with Plessey's SP4632 and has differential outputs.

- 1.1 GHz Toggle Frequency
- Low-Power: 25 mA Typical @ V_{CC} = 5.0 V
- High Input Sensitivity
- 800 mV Minimum Peak-Peak Output Swing
- This Product Preview's Specifications are Design Goals Only

MECL PLL COMPONENTS

LOW-POWER PRESCALER ÷64



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

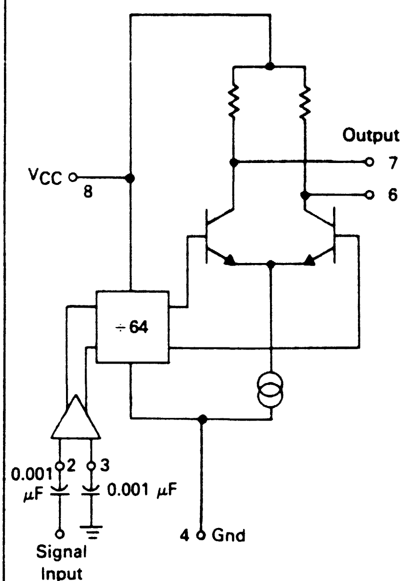
ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}	1.1	—	—	GHz
Supply Current	I_{CC}	—	25	—	mA
Output Voltage (Load = 10 pF, I_{sink} = 200 μA)	V_{out}	0.8	1.0	—	V_{pp}
Input Voltage Sensitivity	$V_{in\ Min}$	—	10	—	mV_{rms}
Input Overload	$V_{in\ Max}$	200	—	—	mV_{rms}
AC Input Resistance	R_{in}	—	TBD*	—	kΩ
Input Capacitance	C_{in}	—	TBD*	—	pF

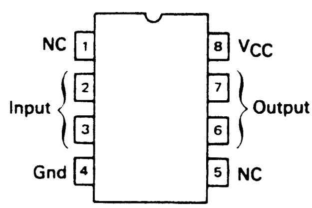
*To be determined.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PRESCALER BLOCK DIAGRAM



PRESCALER PINOUT



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MOTOROLA

MC12074

Product Preview

÷256 LOW-POWER PRESCALER

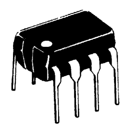
The MC12074 is a new member of Motorola's PLL family. It is a high-speed, low-power prescaler which divides by 256. The MC12074 can be used in all frequency synthesis applications. Typical applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included in the MC12074. This preamplifier isolates the differential inputs and provides gain for the input signal. The MC12074 is pin compatible with Plessey's SP4653 and has differential outputs.

- 1.1 GHz Toggle Frequency
- Low-Power: 25 mA Typical @ V_{CC} = 5.0 V
- High Input Sensitivity
- 800 mV Minimum Peak-Peak Output Swing
- This Product Preview's Specifications are Design Goals Only

MECL PLL COMPONENTS

LOW-POWER PRESCALER ÷256



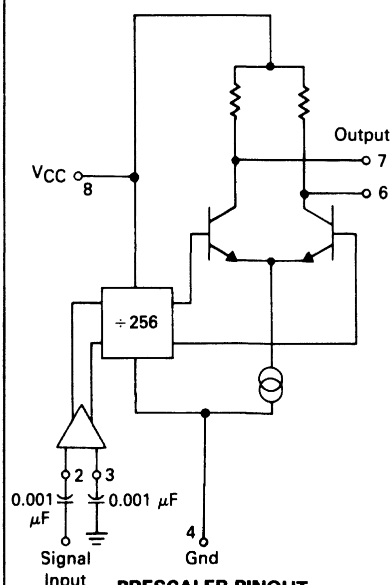
P SUFFIX
PLASTIC PACKAGE
CASE 626

5

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

PRESCALER BLOCK DIAGRAM

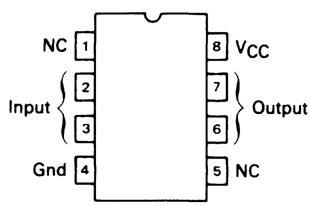


ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}	1.1	—	—	GHz
Supply Current	I_{CC}	—	25	—	mA
Output Voltage (Load = 10 pF, I_{sink} = 200 µA)	V_{out}	0.8	1.0	—	V_{pp}
Input Voltage Sensitivity	$V_{in\ Min}$	—	10	—	mV_{rms}
Input Overload	$V_{in\ Max}$	200	—	—	mV_{rms}
AC Input Resistance	R_{in}	—	TBD*	—	kΩ
Input Capacitance	C_{in}	—	TBD*	—	pF

*To be determined.

PRESCALER PINOUT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC12090

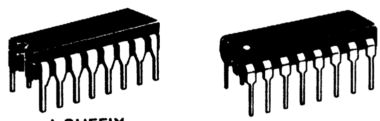
Advance Information

UHF PRESCALER

The MC12090 is a high-speed D master-slave flip-flop capable of toggle rates of over 700 MHz. It was designed primarily for high-speed prescaling applications in communications and instrumentation. This device employs two data inputs, two clock inputs as well as complementary Q and $\overline{Q}$ outputs. There are no SET or RESET inputs.

PLL COMPONENTS

HIGH-SPEED PRESCALER



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

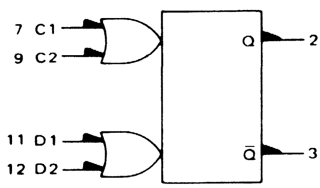
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	65	—	59	—	65	mA
Input Current High	I_{inH}							μA
Pin 7, 9		—	400	—	260	—	260	
Pin 11, 12		—	435	—	280	—	280	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.70	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.87	-1.495	-1.85	-1.48	-1.83	-1.45	Vdc

AC PARAMETERS

Characteristic	Symbol	0°C		25°C		75°C		Unit
		Min	Max	Min	Max	Min	Max	
Toggle Frequency	f_{tog}	700	—	750	—	700	—	MHz
		Typical (25°C)						
Propagation Delay (Clock to Output Pins 7 & 9→2)	t_{pd}	1.3						ns
Setup Time	t_s							ns
$t_{setup\,H}$		0.3						
$t_{setup\,L}$		0.3						
Hold Time	t_h							ns
$t_{hold\,H}$		0.2						
$t_{hold\,L}$		0.3						
Rise Time	t_r	0.9						ns
Fall Time	t_f	0.9						ns

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

C	D	Q_{n+1}
L	φ	Q_n
H	φ	Q_n
↑	L	L
↑	H	H

C = C1 + C2 φ = Don't Care
D = D1 + D2

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI-705

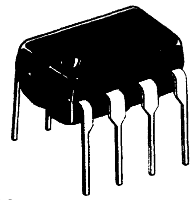
MOTOROLA

MC1376

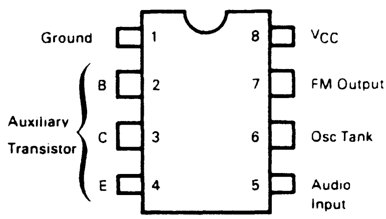
Advance Information

FM MODULATOR CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUIT



CASE 626



FM MODULATOR CIRCUIT

. . . a voltage-controlled oscillator/modulator ideally suited to cordless telephone and television intercarrier applications.

- Wide Supply Range (5.0-12 Vdc)
- Useful Frequency Range (1.4-14 MHz)
- Low Distortion (<1%)
- Excellent Oscillator Stability
- Output RF Driver Transistor Included
- Low Cost, Low Component Count Circuit
- Wide Deviation Capability

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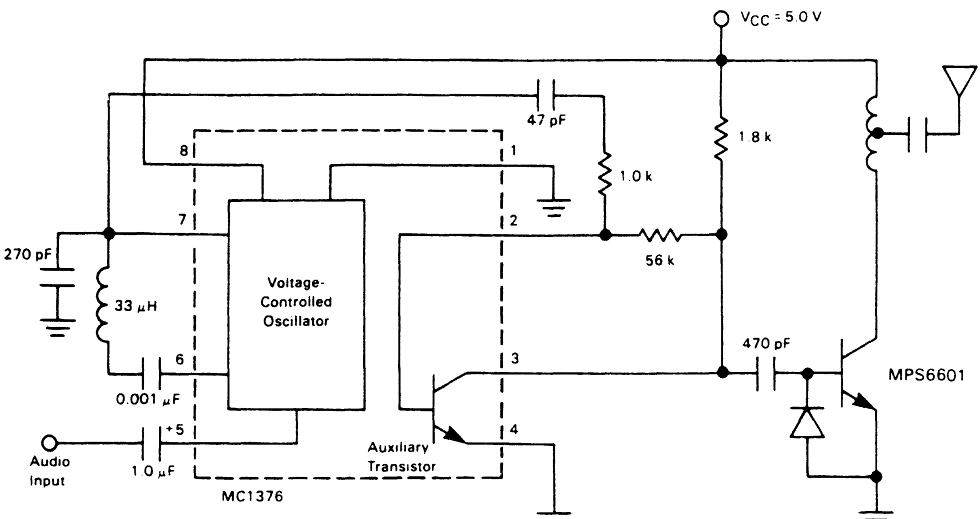
FIGURE 1 — CORDLESS TELEPHONE BASE STATION TRANSMITTER (1.76 MHz)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC14046B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

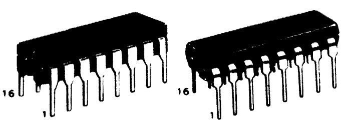
PHASE-LOCKED LOOP

PHASE-LOCKED LOOP

The MC14046B phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90^{o} phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals $PC2_{out}$ and PCP_{out}, and maintains a 0^{o} phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

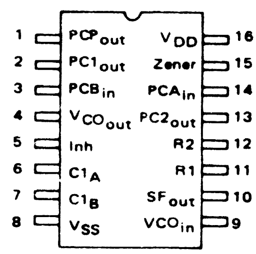
- VCO Frequency = 1.4 MHz Typical @ V_{DD} = 10 Vdc
- VCO Frequency Drift with Temperature = 0.04%/°C Typical @ V_{DD} = 10 Vdc
- VCO Linearity = 1% Typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Dynamic Power Dissipation — 70 μW Typical @ f_0 = 10 kHz, V_{DD} = 5.0 Vdc, R1 = 1.0 MΩ, R2 = ∞, R_{SF} = ∞
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 Vdc
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited



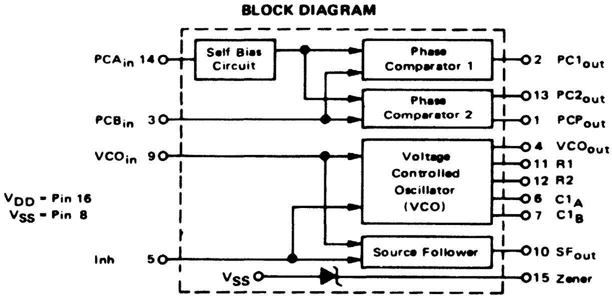
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Pins 6, 7, 10, 11, 12, and 15 if unused must be left open.

DL 130

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MOTOROLA

MC145106

PLL FREQUENCY SYNTHESIZER

The MC145106 is a phase locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for the oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. The circuit provides a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

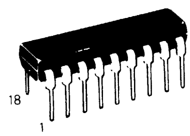
The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal is provided from the on-chip lock detector with a "0" level for the out of lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24 MHz Crystal Oscillator
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (including ÷ 2)
- Three-State Phase Detector
- Pin-for-Pin Replacement for MM55106, MM55116
- Chip Complexity: 880 FETs or 220 Equivalent Gates

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

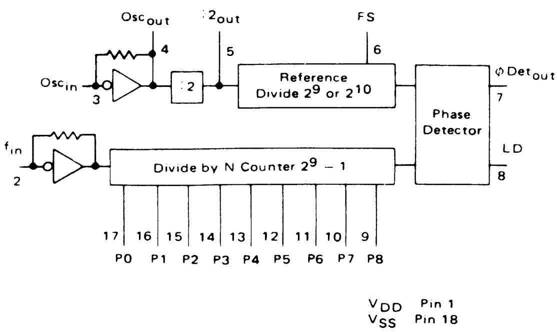
PLL
FREQUENCY SYNTHESIZER



P SUFFIX
PLASTIC PACKAGE
CASE 707

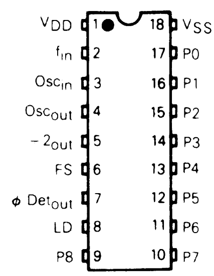
5

BLOCK DIAGRAM



V_{DD} Pin 1
V_{SS} Pin 18

PIN ASSIGNMENT



DL 130

MOTOROLA

MC145145

Advance Information

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145145 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

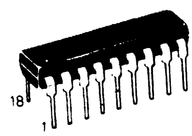
The MC145145 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital-phase detector, 14-bit programmable divide-by-N counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145145 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145145.

- General Purpose Applications
  - CATV
  - AM/FM Radios
  - Two Way Radios
  - TV Tuning
  - Scanning Receivers
  - Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @5 Vdc
- Programmable Reference Divider for Values Between 3 and 4095
- On- or Off-Chip Reference Oscillator Operation
- Single Modulus 4-Bit Data Bus Programming
- ÷N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options —
  - Single Ended (Three State)
  - Double Ended

CMOS LSI

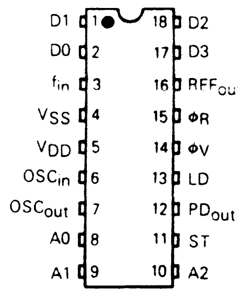
(LOW-POWER COMPLEMENTARY MOS)

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER



P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



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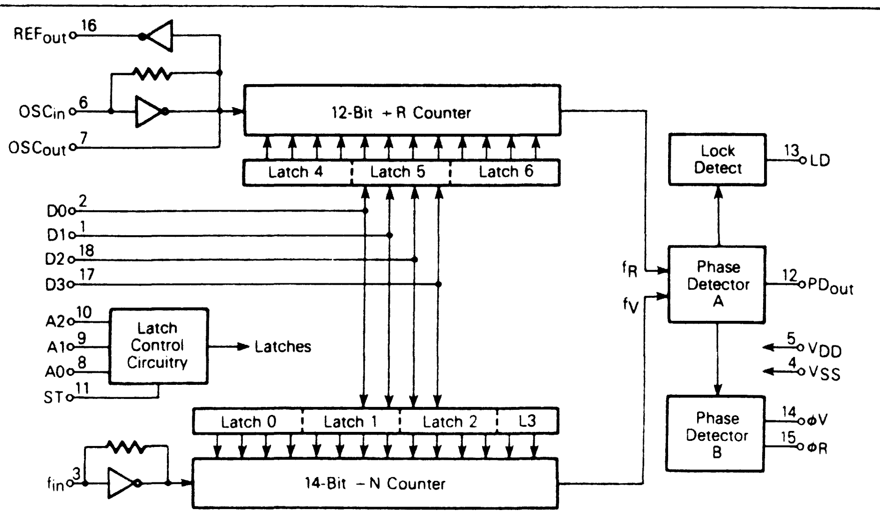


MOTOROLA

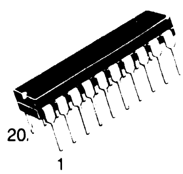
MC145146

Advance Information

CMOS LSI

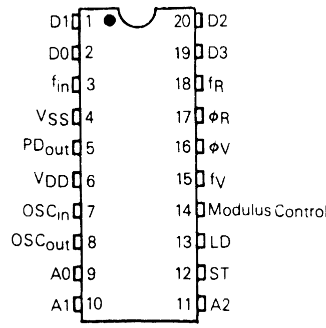
(LOW-POWER COMPLEMENTARY MOS)

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN ASSIGNMENT



4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145146 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

The MC145146 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit divide-by-A counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145146 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and the MC145146

- General Purpose Applications

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two Way Radios	Amateur Radio

- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @5 Vdc
- Programmable Reference Divider for Values Between 3 and 4095
- On- or Off-Chip Reference Oscillator Operation
- Dual Modulus 4-Bit Data Bus Programming
- ÷N Range = 3 to 1023, ÷A Range = 3 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options —
  Single Ended (Three State)
  Double Ended

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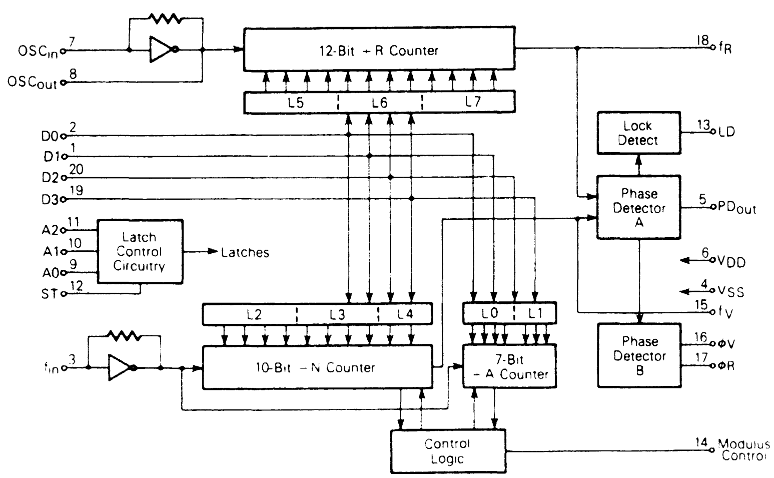


MOTOROLA

MC145155

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145155 is one of a family of LSI PLL Frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

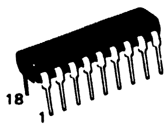
The MC145155 is programmed by a clocked, serial input, 16-bit data steam. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 14-bit programmable divide-by-N counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145155 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145155.

- General Purpose Applications —
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two-Way Radios — Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values — 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Single Modulus/Serial Programming
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options —
  Single Ended (Three-State)
  Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

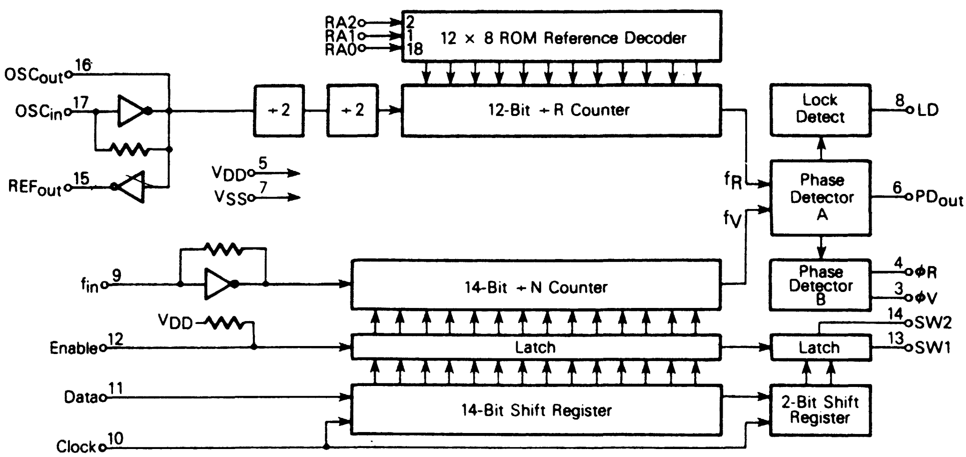


P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT

Pin	Name	Name	Pin
1	RA1	RA0	18
2	RA2	OSC_{in}	17
3	ϕV	OSC_{out}	16
4	ϕR	REF_{out}	15
5	V_{DD}	SW2	14
6	PD_{out}	SW1	13
7	V_{SS}	Enable	12
8	LD	Data	11
9	f_{in}	Clock	10

5



MOTOROLA

MC145156

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145156 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

The MC145156 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable ÷ A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156.

- General Purpose Applications –

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two-Way Radios	Amateur Radio

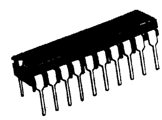
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values – 8, 64, 128, 256, 640, 1000, 1024, 2048
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- ÷N Range = 3 to 1023
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options –
  Single Ended (Three-State)
  Double Ended

5

CMOS LSI

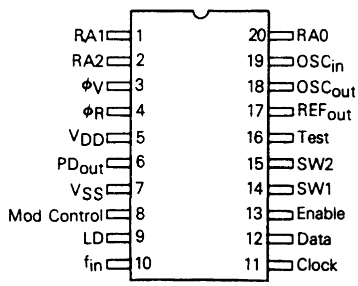
(LOW-POWER COMPLEMENTARY MOS)

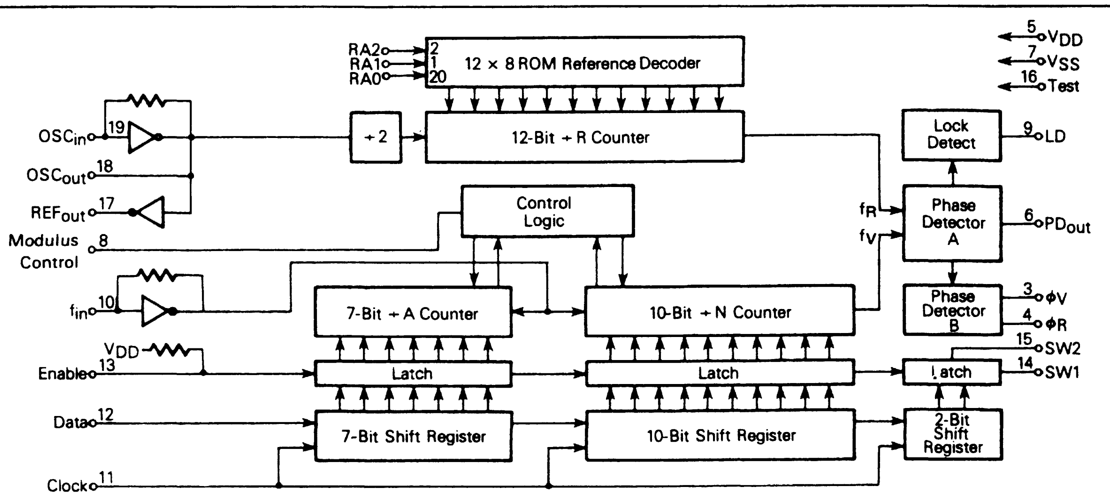
SERIAL INPUT PLL FREQUENCY SYNTHESIZER



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN ASSIGNMENT





Reprint December 1983

![MOTOROLA]

MOTOROLA

MC145157
MC145158

Advance Information

SERIAL INPUT PLL FREQUENCY SYNTHESIZERS

The MC145157 and MC145158 are part of a family of CMOS Phase Lock Loop frequency synthesizer devices from Motorola. These devices utilize silicon-gate CMOS technology to achieve the operating speeds necessary for high-frequency operation. The family includes devices having serial, parallel, and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, and a choice of phase detector types.

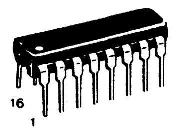
The MC145157 and MC145158 have fully programmable 14-bit reference counters, as well as fully programmable ÷ N (MC145157) and ÷ N/÷ A (MC145158) counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

When combined with a loop filter and VCO, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed-divide prescaler can be used between the VCO and the PLL for the MC145157 and a dual-modulus prescaler for the MC145158.

- General Purpose Applications –
  CATV
  AM/FM Radios
  Two-Way Radios
  TV Tuning
  Scanning Receivers
  Amateur Radio
- Low Power Drain
- 3.0 to 9.0 V Supply Range
- 30 MHz Typical Input Capability @ 5 V (f_{in} Input)
- Fully Programmable Reference and ÷ N Counters
- Reference Divider Range = 3 to 16383
- ÷ N Range = 3 to 16383 for the MC145157
- Dual Modulus Capability for the MC145158
- f_V and f_r Outputs
- Lock Detect Signal
- "Linearized" Digital Phase Detector
- Single Ended (Three-State) or Double-Ended Phase Detector Outputs

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT PLL FREQUENCY SYNTHESIZER



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXX

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
C	Limited Operating Temperature Range

5

PIN ASSIGNMENT

MC145157

Pin	Name	Pin	Name
1	OSC_{in}	16	ϕR
2	OSC_{out}	15	ϕV
3	f_V	14	REF_{out}
4	V_{DD}	13	f_R
5	PD_{out}	12	S/R_{out}
6	V_{SS}	11	LE
7	LD	10	Data
8	f_{in}	9	Clock

MC145158

Pin	Name	Pin	Name
1	OSC_{in}	16	ϕR
2	OSC_{out}	15	ϕV
3	f_V	14	REF_{out}
4	V_{DD}	13	f_R
5	PD_{out}	12	Modulus Control
6	V_{SS}	11	LE
7	LD	10	Data
8	f_{in}	9	Clock

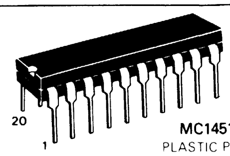
MOTOROLA

MC145159-1

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH ANALOG PHASE DETECTOR



MC145159P1
PLASTIC PACKAGE
CASE 738

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH ANALOG PHASE DETECTOR

The MC145159-1 has a programmable 14-bit reference counter, as well as programmable divide-by-N/divide-by-A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

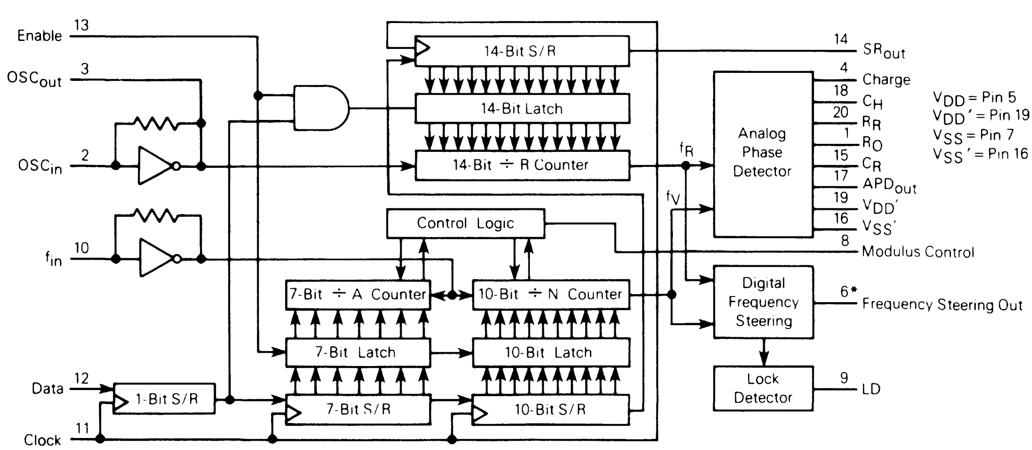
When combined with a loop filter and VCO, this device can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operations, a down mixer or a dual modulus prescaler can be used between the VCO and the PLL.

- General Purpose Applications:
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two Way Radios — Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Dual Modulus
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- ÷ R Range = 3 to 16383
- ÷ N Range = 16 to 1023, ÷ A Range = 0 to 127
- High-Gain Analog Phase Detector

5

PIN ASSIGNMENT

Name	Pin	Pin	Name
R_O	1	20	R_R
OSC_{in}	2	19	V_{DD}'
OSC_{out}	3	18	C_H
Charge	4	17	APD_{out}
V_{DD}	5	16	V_{SS}'
Frequency Steering Out	6	15	C_R
V_{SS}	7	14	SR_{out}
Modulus Control	8	13	Enable
LD	9	12	Data
f_{in}	10	11	Clock



*Note: Pin 6 is not and cannot be used as a digital phase detector output.

MOTOROLA

MC145160
MC145161

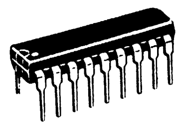
Product Preview

DUAL PLL

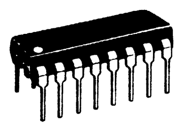
The MC145160 is a dual phase locked loop frequency synthesizer intended for use primarily in 46/49 MHz cordless phone. The part contains two ROM programmable counters for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider is shared by the receive and transmit circuits.

Other features include a lock detect circuit for the transmit loop, illegal code default, a buffered oscillator output for mixing purposes in the system, 5 KHz and 4 KHz tone output. The reference oscillator can also be optioned to accept an 11.15 MHz crystal.

- FCC 46/49 MHz Cordless Phone Channel ROM
- On-chip PLL for transmit/receive
- On-chip Oscillator with Buffered Output
- Low Power Consumption
- 3.0 to 5.5V Supply Range
- Lock Detect Signal
- 5 KHz/4 KHz Output



CASE 707-02
PLASTIC



CASE 648
PLASTIC

5

PIN ASSIGNMENT

OSCout	1	18	OSC IN
MODE	2	17	VDD
$\overline{SB}$	3	16	Fin 1
5 K	4	15	OSC B
4 K	5	14	PD1
D0	6	13	VSS
D1	7	12	PD2
D2	8	11	LD
D3	9	10	Fin 2

MC145160

OSCout	1	16	OSC in
MODE	2	15	VDD
$\overline{SB}$	3	14	Fin 1
5 K	4	13	PD1
D0	5	12	VSS
D1	6	11	PD2
D2	7	10	LD
D3	8	9	Fin 2

MC145161

MOTOROLA

MC145163

ADVANCE INFORMATION

BCD INPUT PLL FREQUENCY SYNTHESIZER

This is one of a family of LSI PLL frequency synthesizer parts from MOTOROLA CMOS. The family includes devices having serial, parallel, 4-bit data bus and BCD programmable inputs.

This is programmed by 4 digit BCD inputs. The device features consist of a reference oscillator, selectable reference divider, two output phase detectors and a 4 digit BCD programmable divided-by-N counter.

- General Purpose Applications
  - Two-Way Radio
  - Amateur Radio
  - Industrial Receiver
- Low Power Consumption
- 3.0 to 9.0 Vdc Supply Range
- > 30 MHz Typical Input Capability @ 5 Vdc
- On or Off - Chip Reference Oscillator Operation
- Lock Detect Signal
- 4 User - Selectable ÷ R Value - 512, 1024, 2048, 4096
- ÷ N Range = 3 to 9999
- 'Linearized' Digital Phase Detector Enhances Transfer Function linearity
- Two Error Signal Options: Single Ended (Three-State)
  Double Ended

C SUFFIX
PLASTIC
QUAD PACKAGE

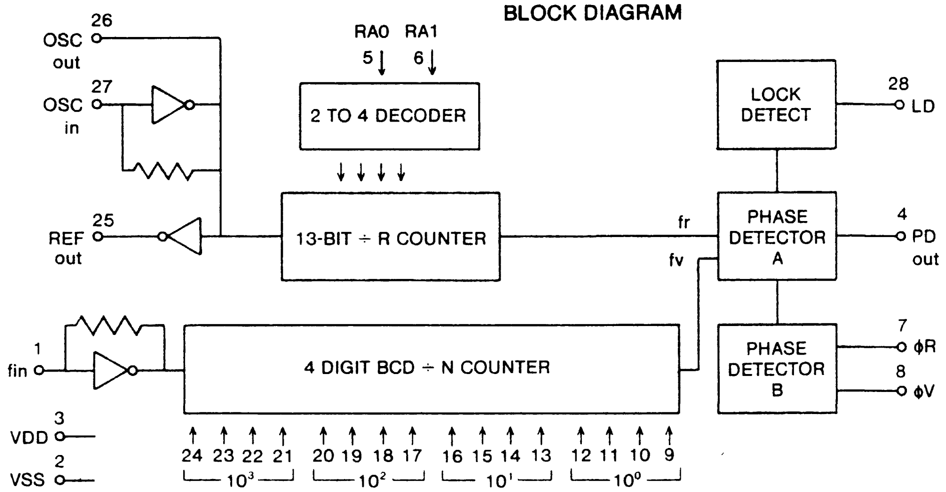
P SUFFIX
PLASTIC
DIL PACKAGE
CASE 710

PIN ASSIGNMENT (P SUFFIX)

1	Fin	LD	28
2	VSS	OSCin	27
3	VDD	OSCout	26
4	PDout	REFout	25
5	RA0	D3D	24
6	RA1	D3C	23
7	φR	D3B	22
8	φV	D3A	21
9	D0A	D2D	20
10	D0B	D2C	19
11	D0C	D2B	18
12	D0D	D2A	17
13	D1A	D1D	16
14	D1B	D1C	15

5

BLOCK DIAGRAM



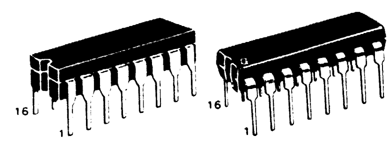
MOTOROLA

MC14568B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS



L SUFFIX	P SUFFIX
CERAMIC PACKAGE	PLASTIC PACKAGE
CASE 620	CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

5

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

The MC14568B consists of a phase comparator, a divide-by-4, 16, 64 or 100 counter and a programmable divide-by-N 4-bit binary counter (all positive-edge triggered) constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

The MC14568B has been designed for use in conjunction with a programmable divide-by-N counter for frequency synthesizers and phase-locked loop applications requiring low power dissipation and/or high noise immunity.

This device can be used with both counters cascaded and the output of the second counter connected to the phase comparator (CTL high), or used separate of the programmable divide-by-N counter, for example cascaded with MC14569B (CTL low), MC14522B or MC14526B.

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

TRUTH TABLE

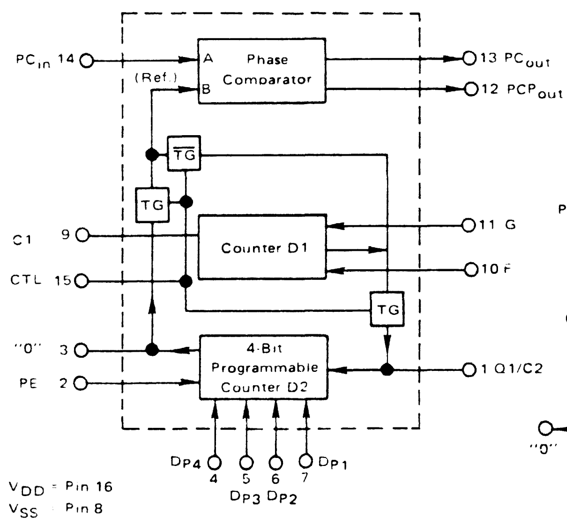
F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

The divide-by-zero state on the programmable divide-by-N 4-bit binary counter, D2, is illegal.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

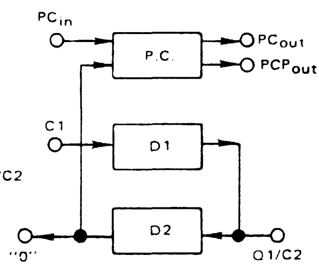
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM

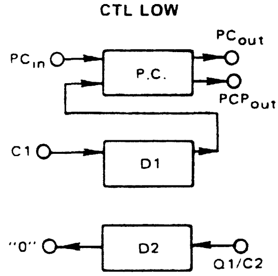


V_{DD} = Pin 16
V_{SS} = Pin 8

CTL HIGH



CTL LOW



ORDERING INFORMATION

Device	Temperature Range	Package
MC1496G	0°C to +70°C	Metal Can
MC1496L	0°C to +70°C	Ceramic DIP
MC1496P	0°C to +70°C	Plastic DIP
MC1596G	−55°C to +125°C	Metal Can
MC1596L	−55°C to +125°C	Ceramic DIP

MC1496
MC1596

Specifications and Applications Information

BALANCED MODULATOR — DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  – 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

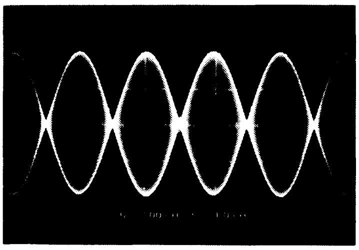


FIGURE 1 – SUPPRESSED-CARRIER OUTPUT WAVEFORM

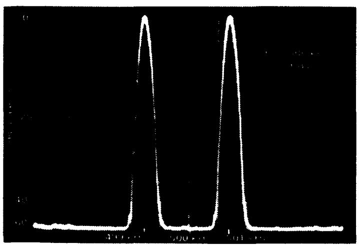


FIGURE 2 – SUPPRESSED-CARRIER SPECTRUM

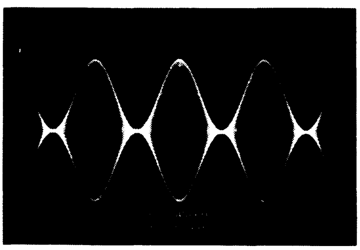
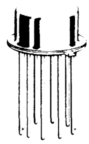
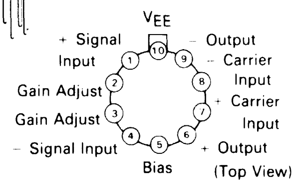
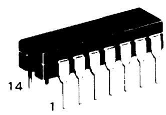


FIGURE 3 – AMPLITUDE-MODULATION OUTPUT WAVEFORM

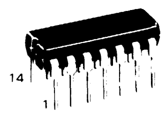


G SUFFIX
METAL PACKAGE
CASE 603-04





L SUFFIX
CERAMIC PACKAGE
CASE 632-02



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

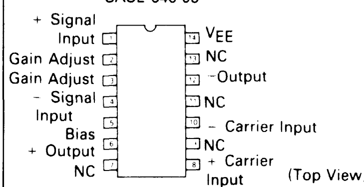
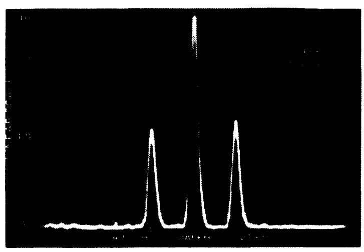


FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM



5

DS9132

MOTOROLA

MC2831A

Advance Information

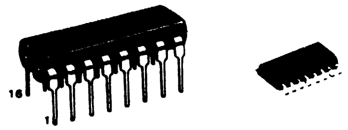
LOW POWER FM TRANSMITTER SYSTEM

MC2831A is one chip FM transmitter system designed for cordless phone and FM communication equipments. It includes Mic Amplifier, Pilot Tone Oscillator, Voltage Controlled Oscillator and Battery Checker.

- Wide range of operating supply voltage (3.0V–8.0V)
- Low drain current (4.0mA typ full operation at V_{CC} = 4.0V)
- Battery checker (290 μA typ at V_{CC} = 4.0V)
- Low number of external parts required

LOW POWER FM TRANSMITTER SYSTEM

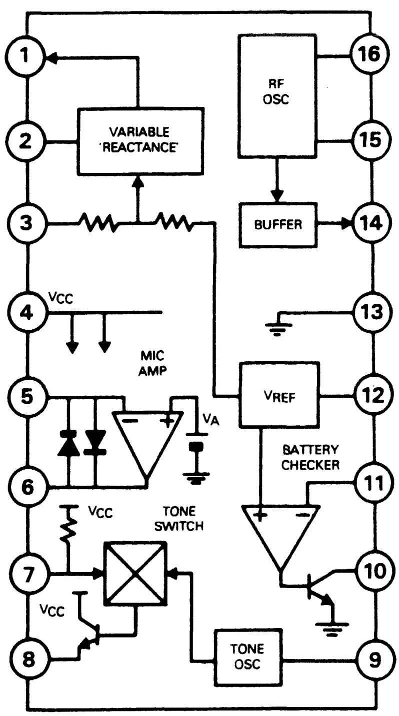
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
SOIC
CASE 751 B

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



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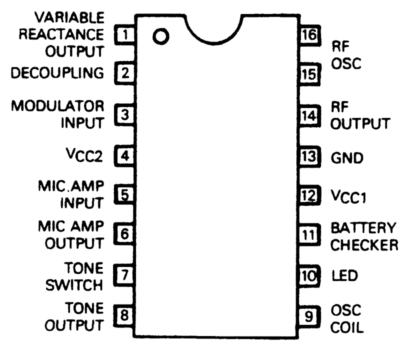
PIN CONNECTIONS



MOTOROLA

MC3356

Advance Information

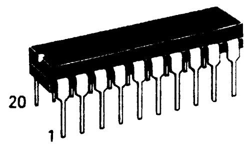
WIDEBAND FSK RECEIVER

. . . includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communications equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: −3 dB Limiting Sensitivity 30 μVrms @ 100 MHz
- Highly versatile, full-function device, yet few external parts are required

WIDEBAND FSK RECEIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738

5

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

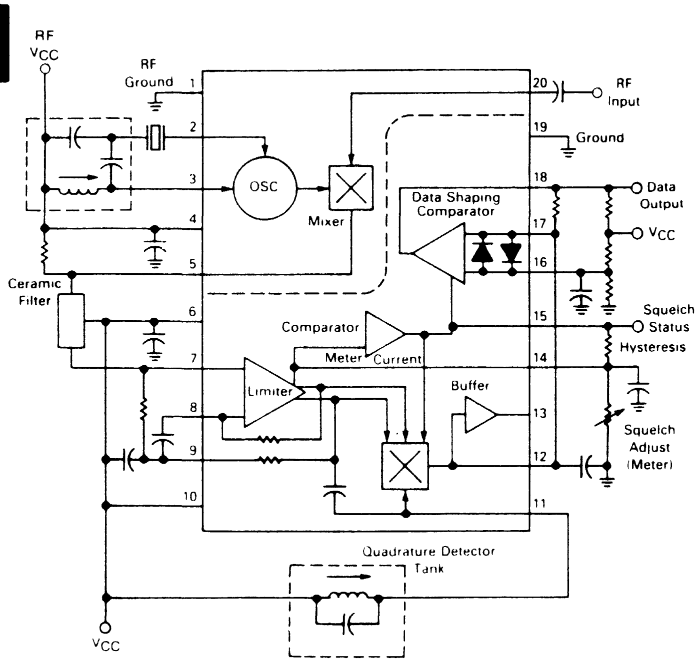
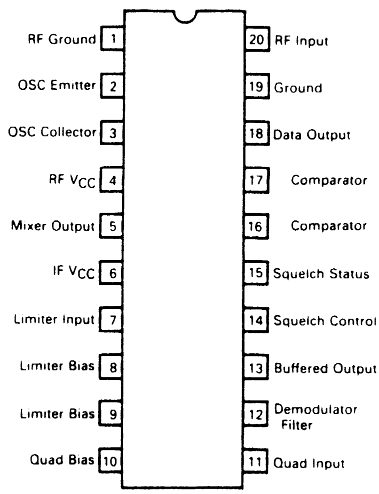


FIGURE 2 — PIN CONNECTIONS



MOTOROLA

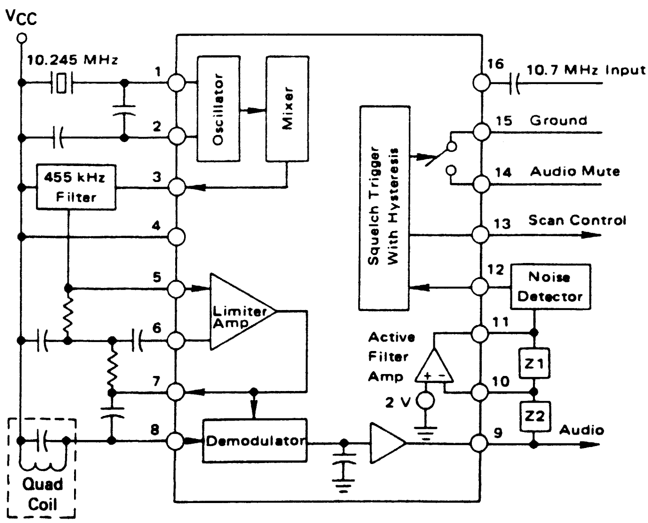
MC3357

LOW POWER NARROW BAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

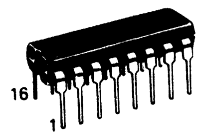
- Low Drain Current (3.0 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage – (-3.0 dB) = 5.0 μV (Typ)
- Low Number of External Parts Required

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

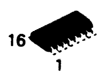


LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



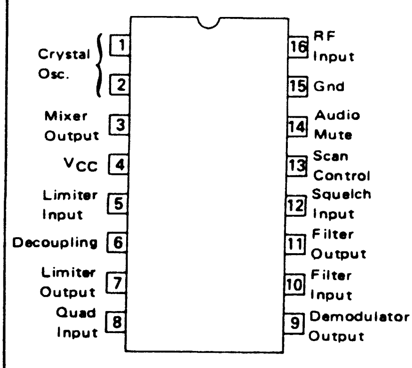
P SUFFIX
PLASTIC PACKAGE
CASE 648-05



D SUFFIX
PLASTIC PACKAGE
CASE 751B-01
SO-16

5

PIN CONNECTIONS



MOTOROLA

MC3359

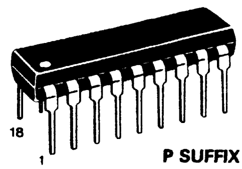
HIGH-GAIN LOW-POWER FM IF

MONOLITHIC SILICON INTEGRATED CIRCUIT

LOW-POWER NARROW-BAND FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrow-band FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts.

- Low Drain Current (3.6 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (−3.0 dB) = 2.0 μV (Typ)
- Low Number of External Parts Required



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P SUFFIX
PLASTIC PACKAGE
CASE 701-01

FIGURE 1 — TYPICAL APPLICATION IN A SCANNER RECEIVER

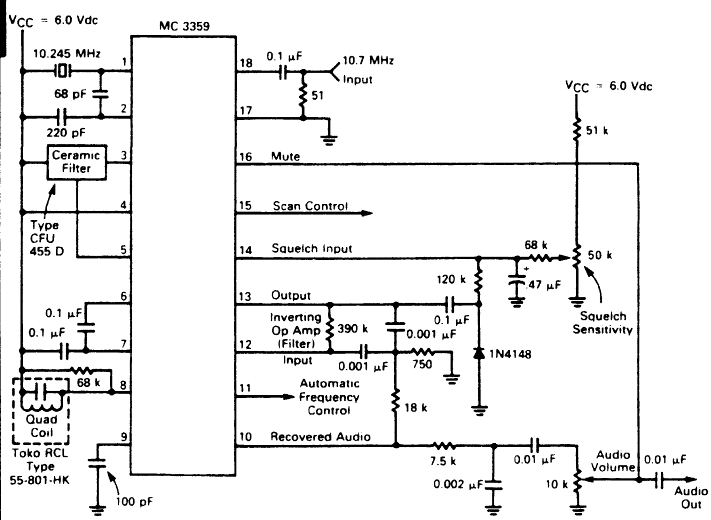
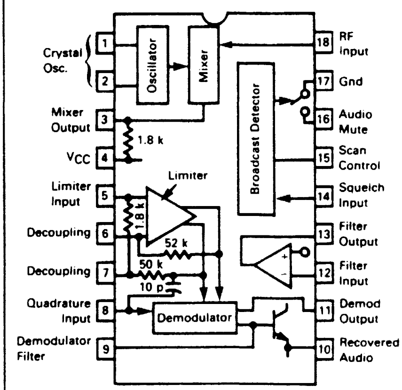


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



5

MOTOROLA

MC3361A

Advance Information

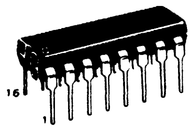
LOW POWER NARROW BAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3361A is designed for use in FM dual conversion communications equipment.

- Operates From 2.0 V to 8.0 V Supply
- Low Drain Current 4.2 mA Typ @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage— −3.0 dB = 2.0 μV Typ
- Low Number of External Parts Required
- Operating Frequency Up to 60 MHz

LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648-05

D SUFFIX
SOIC
CASE 751B

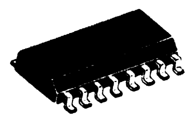
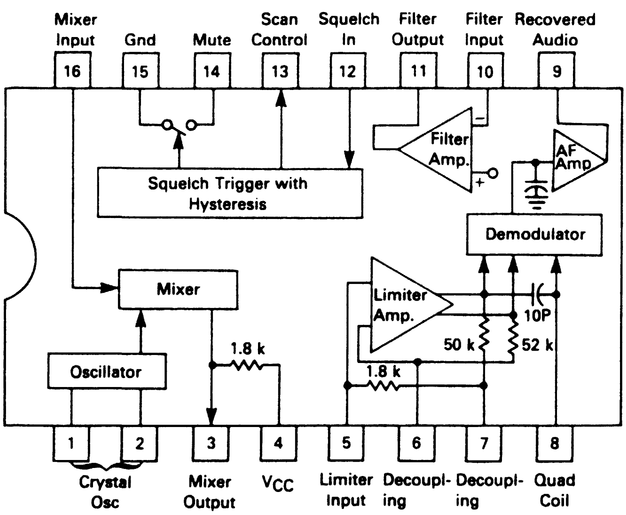
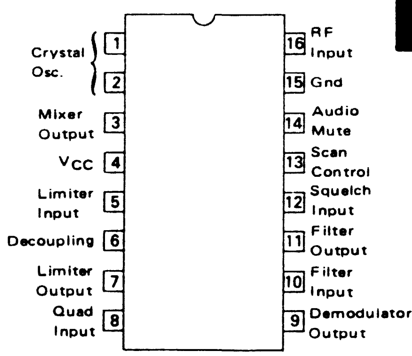


FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



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1-1986

MOTOROLA

MC3362/63

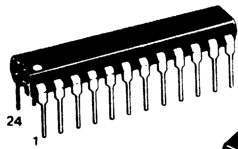
Product Preview

RECEIVER I.C.

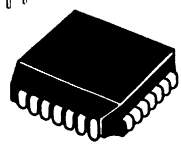
FEATURES

- Single Supply Operation from 2-7 VDC
- Low Power Consumption (3mA at 2 V Typ)
- RF Input Frequency Response to over 50 MHz at V_{CC} = 2 V
- Doubly Balanced First Mixer
- First LO configurable as XCO or VCO with On Board Tuning Diodes
- Wide Dynamic Range Signal Strength Indicator with Externally Set Threshold
- Data Slicer detects Zero Crossings of FSK Modulation of Carrier
- Available in Full Function 28 Pin Quad (Surface Mount) or 24 Pin DIN Packages

PACKAGING & PIN OUT*

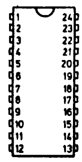


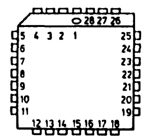
P SUFFIX
PLASTIC PACKAGE
CASE 724-02



PLASTIC QUAD
SURFACE MOUNT
CASE 776-01

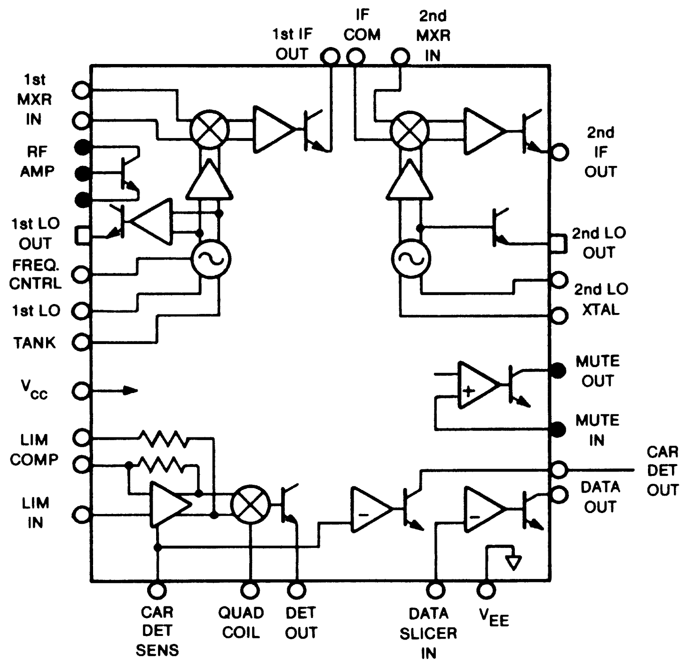
MC3362





MC3363

MC3362/63 RECEIVER I.C. INTERNAL BLOCK DIAGRAM



PIN OPTIONS
□ ONLY AVAILABLE ON 24 PIN DIP, MC3362
● ONLY AVAILABLE ON 28 PIN QUAD, MC3363

*PACKAGING SUBJECT TO CHANGE

MOTOROLA

MC3393P

Advance Information

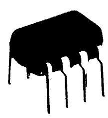
TWO MODULUS PRESCALER

The MC3393P can divide by 15 and 16, and can be used with Motorola CMOS frequency synthesizers MC145146, 52, 56 for commercial AM-FM radio, land mobile and marine two-way radios, avionic radios, and scanner receivers.

- 140 MHz (typ) Toggle Frequency
- ÷15/16
- TTL and CMOS Compatible Output
- Active Pullup and Pulldown
- +5.0 V Supply
- Buffered Clock Input
- 100–400 mV (typ) Input Sensitivity
- 200 Milliwatts (typ)

TWO MODULUS PRESCALER

SILICON MONOLITHIC INTEGRATED CIRCUIT



N SUFFIX
PLASTIC PACKAGE
CASE 626-04

5

FIGURE 1 — LOGIC DIAGRAM

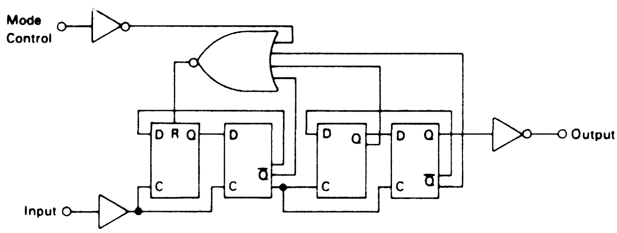
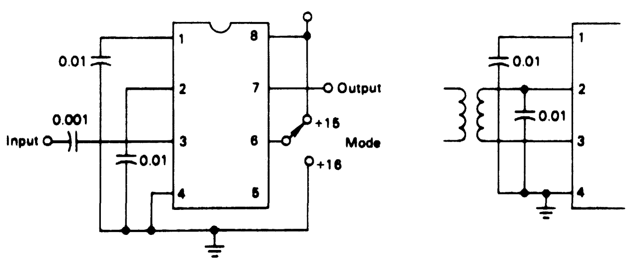


FIGURE 2 — TEST CIRCUITS



Capacitor Coupled Input

Link Coupled Input

Pin Outs
1. Bias Decouple
2. Bias Decouple
3. Input
4. Ground
5. NC
6. Input
7. Output
8. V_{CC}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC3396P

Advance Information

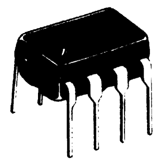
DIVIDE BY 20 PRESCALER

SILICON MONOLITHIC INTEGRATED CIRCUIT

DIVIDE BY 20 PRESCALER

The MC3396P is a fixed ÷20 prescaler for use in frequency synthesizers and similar applications.

- 200 MHz (typ) Toggle Frequency
- Single 5.0 Volt Supply
- Buffered Clock Input
- 100 mV — 400 mV RMS Input Sensitivity
- Open Collector Saturating Output is Capable of Driving TTL and CMOS.



P SUFFIX
PLASTIC PACKAGE
CASE 626

5

FIGURE 1 — LOGIC DIAGRAM

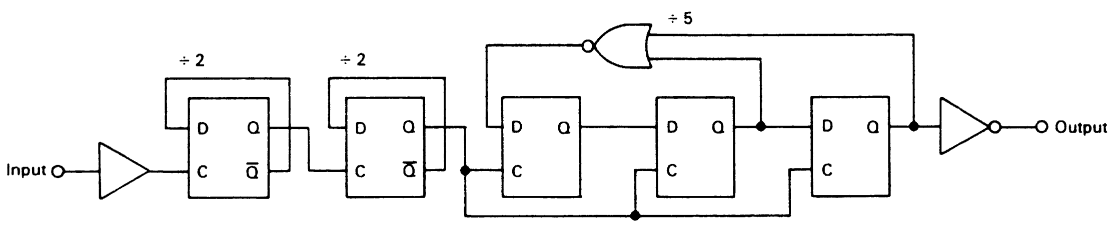
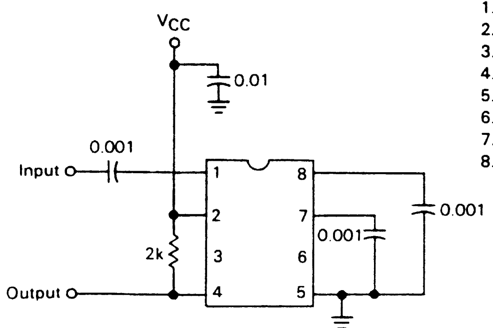


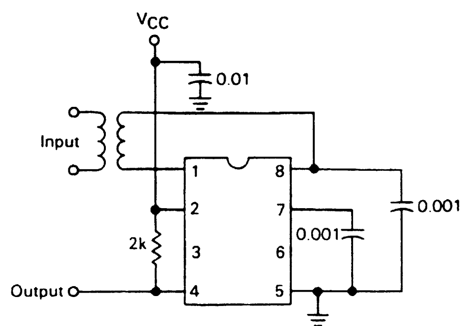
FIGURE 2 — CAPACITOR-COUPLED INPUT



PIN CONNECTIONS

1. Input
2. V_{CC}
3. NC
4. Output
5. Ground
6. NC
7. Bias Decouple
8. Bias Decouple

FIGURE 3 — LINK-COUPLED INPUT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

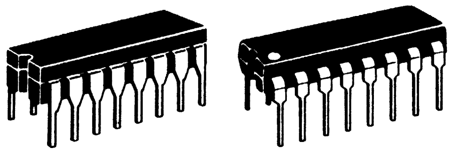
MC4316 • MC4016
MC4317 • MC4017
MC4318 • MC4018
MC4319 • MC4019

PROGRAMMABLE MODULO-N COUNTERS

The monolithic devices are programmable, cascadable, modulo-N-counters. The MC4316/4016 can be programmed to divide by any number (N) from 0 thru 9, the MC4318/4018 from 0 thru 15. The MC4317/4017 consists of a modulo 2 counter which can be programmed to divide by 0 or 1 and a modulo 5 counter which can be programmed to divide by any number from 0 to 4. The MC4319/4019 contains two modulo 4 counters.
which can be programmed to divide by any number from 0 to 3.

The parallel enable ($\overline{PE}$) input enables the parallel data inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.



L SUFFIX
CERAMIC PACKAGE
CASE 620

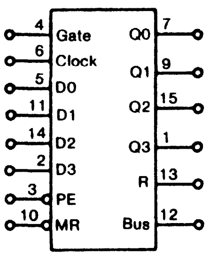
P SUFFIX
PLASTIC PACKAGE
CASE 648
MC4016 thru MC4019
only

All Types:

Input Loading Factor:
Clock, $\overline{PE}$ = 2
D0, D1, D2, D3, Gate = 1
$\overline{MR}$ = 4
Output Loading Factor = 8

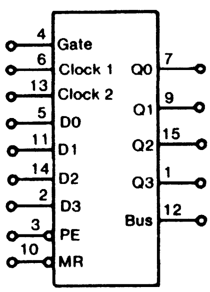
Total Power Dissipation =
250 mW typ/pkg
Propagation Delay Time:
Clock to Q3 = 50 ns typ
Clock to Bus = 35 ns typ

MC4316/4016
MC4318/4018



V_{CC} = Pin 16
Gnd = Pin 8

MC4317/4017
MC4319/4019



V_{CC} = Pin 16
Gnd = Pin 8

MC4316/4016

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC4318/4018

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC4317/4017

COUNT	OUTPUT
	Q0
1	1
0	0

COUNT	OUTPUT		
	Q3	Q2	Q1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

MC4319/4019

COUNT	OUTPUT	
	Q1	Q0
3	1	1
2	1	0
1	0	1
0	0	0

COUNT	OUTPUT	
	Q3	Q2
3	1	1
2	1	0
1	0	1
0	0	0

5

DS 9554R1 (Issue C)

Phase Locked Loop Design Fundamentals (AN535)

6

PHASE-LOCKED LOOP DESIGN FUNDAMENTALS

INTRODUCTION

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

PARAMETER DEFINITION

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s). This response is twofold in nature in that it contains both the transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.[1]

The parameters in Figure 1 are defined and will be used throughout the text.

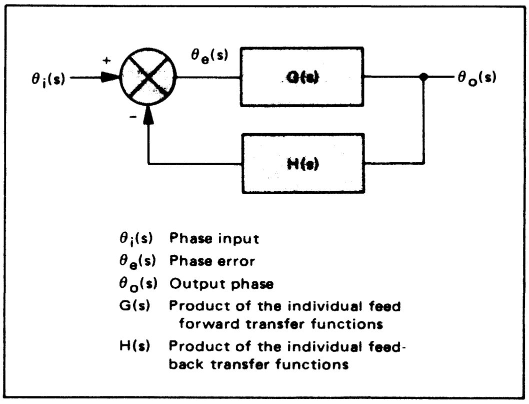


FIGURE 1 – Feedback System

Using servo theory, the following relationships can be obtained.[2]

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\;\theta_i(s) \tag{1}$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s)\,H(s)}\;\theta_i(s) \tag{2}$$

These parameters relate to the functions of a PLL as shown in Figure 2.

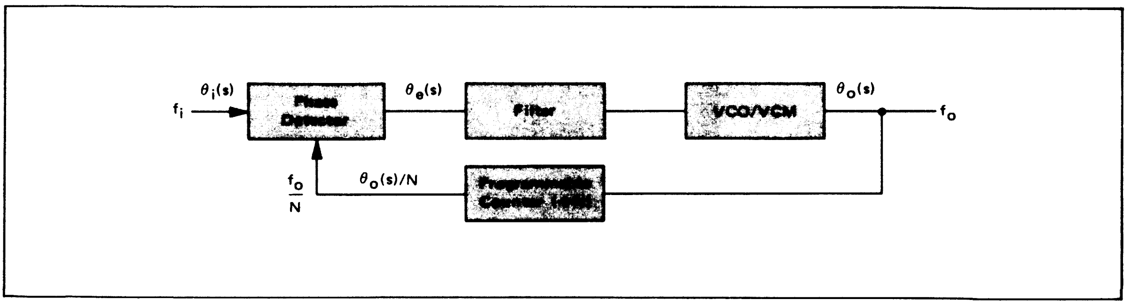


FIGURE 2 – Phase Locked Loop

The phase detector produces a voltage proportional to the phase difference between the signals θ_i and θ_o/N. This voltage upon filtering is used as the control signal for the VCO/VCM (VCM - Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$f_o = N f_i \tag{3}$$

during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path (N = 1). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

TYPE – ORDER

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The type of a system refers to the number of poles of the loop transfer function G(s) H(s) located at the origin. Example:

$$\text{let} \quad G(s)\,H(s) = \frac{10}{s(s+10)} \tag{4}$$

This is a type one system since there is only one pole at the origin.

The order of a system refers to the highest degree of the polynomial expression

$$1 + G(s)\,H(s) = 0 \triangleq \text{C.E.} \tag{5}$$

which is termed the Characteristic Equation (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function.

Example:

$$G(s)\,H(s) = \frac{10}{s(s+10)} \tag{6}$$

then

$$1 + G(s)\,H(s) = 1 + \frac{10}{s(s+10)} = 0 \tag{7}$$

therefore

$$\text{C.E.} = s(s+10) + 10 \tag{8}$$

$$\text{C.E.} = s^2 + 10s + 10 \tag{9}$$

which is a second order polynomial. Thus, for the given G(s) H(s), we obtain a type 1 second order system.

ERROR CONSTANTS

Various inputs can be applied to a system. Typically these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_e(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_o(s)/N$. In evaluating a system, $\theta_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error $\theta_e(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.[3]

Simply stated

$$\lim_{t \to \infty} [\theta(t)] = \lim_{s \to 0} [s\,\theta_e(s)] \tag{10}$$

Where

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\,\theta_i(s) \tag{11}$$

The input signal $\theta_i(s)$ is characterized as follows:

$$\text{Step position:} \quad \theta_i(t) = C_p \quad t \geqslant 0 \tag{12}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_p}{s} \tag{13}$$

where C_p is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by C_p radians:

$$\text{Step velocity:} \quad \theta_i(t) = C_v t \quad t \geqslant 0 \tag{14}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_v}{s^2} \tag{15}$$

where C_v is the magnitude of the rate of change of phase in radians per second. This corresponds to inputing a frequency that is different than the feedback portion of the VCO frequency. Thus, C_v is the frequency difference in radians per second seen at the phase detector.

$$\text{Step acceleration:} \quad \theta_i(t) = C_a t^2 \quad t \geqslant 0 \tag{16}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{2\,C_a}{s^3} \tag{17}$$

C_a is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop G(s) H(s) transfer functions for types 1, 2, and 3 are:

$$\text{Type 1} \quad G(s)\,H(s) = \frac{K}{s(s+a)} \tag{18}$$

6

$$\text{Type 2} \quad G(s)\,H(s) = \frac{K(s+a)}{s^2} \tag{19}$$

$$\text{Type 3} \quad G(s)\,H(s) = \frac{K(s+a)(s+b)}{s^3} \tag{20}$$

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

$$\theta_e(s) = \left(\frac{1}{1 + \dfrac{K}{s(s+a)}}\right)\left(\frac{C_p}{s}\right)$$

$$= \frac{(s+a)\,C_p}{(s^2 + as + K)} \tag{21}$$

$$\theta_e(t=\infty) = \lim_{s \to 0}\left[s\left(\frac{s+a}{s^2+as+K}\right)C_p\right] = 0 \tag{22}$$

Thus the final value of the phase error is zero when a step position (phase) is applied.

Similarly applying the three inputs into type 1, 2 and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

TABLE I – Steady State Phase Errors for Various System Types

	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table I the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

STABILITY

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the characteristic equation) vary with loop gain. For stability all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.[2]

Rule 1 - The root locus begins at the poles of G(s) H(s) (K = 0) and ends at the zeroes of G(s) H(s) ($K = \infty$). Where K is loop gain.

Rule 2 - The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of G(s) H(s).

Rule 3 - The root locus contour is bounded by asymptotes whose angular position is given by

$$\frac{(2n+1)}{\#P - \#Z}\,\pi;\; n = 0, 1, 2, \ldots \tag{23}$$

Where #P (#Z) is the number of poles (zeroes).

Rule 4 - The intersection of the asymptotes is positioned at the center of gravity C. G.

$$\text{C.G.} = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} \tag{24}$$

Where ΣP (ΣZ) denotes the summation of the poles (zeroes).

Rule 5 - On a given section of the real axis, root loci may be found in the section only if the #P + #Z to the right is odd.

Rule 6 - Breakaway points from negative real axis is given by:

$$\frac{dK}{ds} = 0 \tag{25}$$

Again where K is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

$$G(s)\,H(s) = \frac{K}{s(s+4)} \tag{26}$$

The root locus has two branches (Rule 2) which begin at s = 0 and s = –4 and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes the equation becomes:

$$\frac{2n+1}{2}\,\pi = \begin{cases} \dfrac{\pi}{2} & \text{for } n = 0 \\[2ex] \dfrac{3\pi}{2} & \text{for } n = 1 \end{cases} \tag{27}$$

6

The position of the intersection according to the Rule 4 is:

$$s = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} = \frac{(-4 -0) - (0)}{2 - 0}$$

$$s = -2 \qquad (28)$$

The breakaway point as defined by Rule 6 can be found by first writing the characteristic equation.

$$\text{C.E.} = 1 + G(s)\,H(s) = 0$$

$$= 1 + \frac{K}{s(s+4)} = s^2 + 4s + K = 0 \qquad (29)$$

Now solving for K yields

$$K = -s^2 - 4s \qquad (30)$$

Taking the derivative with respect to s and setting it equal to zero then determines the breakaway point.

$$\frac{dK}{ds} = \frac{d}{ds}(-s^2 - 4s) \qquad (31)$$

$$\frac{dK}{ds} = -2s - 4 = 0 \qquad (32)$$

or

$$s = -2 \qquad (33)$$

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

This second order characteristic equation given by Equation 29 has been normalized to a standard form[2]

$$s^2 + 2\zeta\,\omega_n s + \omega_n^2 \qquad (34)$$

where the damping ratio $\zeta = \text{Cos}\,\phi\ (0^\circ \leqslant \phi \leqslant 90^\circ)$ and ω_n is the natural frequency as shown in Figure 3.

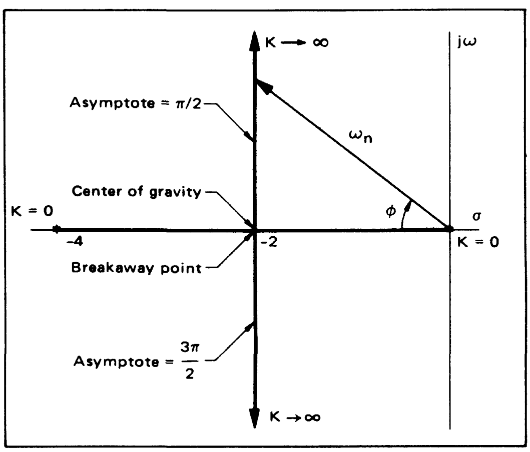


FIGURE 3 – Type 1 Second Order Root Locus Contour

The response of this type 1, second order system to a step input is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

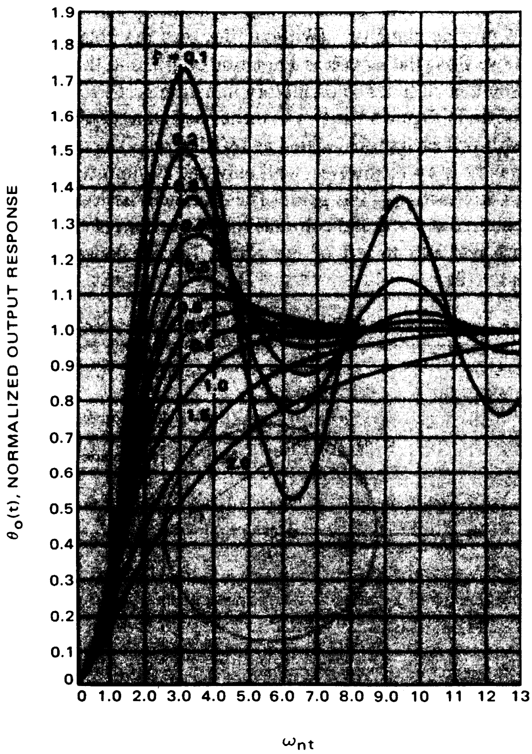


FIGURE 4 – Type 1 Second Order Step Response

The overshoot and stability as a function of the damping ratio ζ is illustrated by the various plots. Each response is plotted as a function of the normalized time $\omega_n t$. For a given ζ and a lock-up time t, the ω_n required to achieve the desired results can be determined. Example:

Assume $\zeta = 0.5$
error $< 10\%$
for $t > 1$ ms

From $\zeta = 0.5$ curve the error is less than 10% of final value for all time greater than $\omega_n t = 4.5$. The required ω_n can then be found by:

$$\omega_n t = 4.5 \qquad (35)$$

or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5\ \text{k rad/s} \qquad (36)$$

ζ is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.

Example:

Another common loop transfer function takes the form

$$G(s)\,H(s) = \frac{(s+a)k}{s^2} \qquad (37)$$

This is a type 2 second order system. A zero is added to provide stability. (Without the zero the poles would move along the $j\omega$ axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is $s = a$; however, with only one asymptote there is no intersection at this point. The root locus lies on a circle centered at $s = -a$ and continues on all portions of the negative real axis to left of the zero. The breakaway point is $s = -2a$.

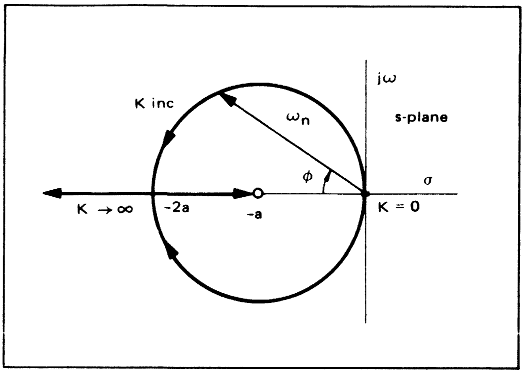


FIGURE 5 – Type 2 Second Order Root Locus Contour

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example the required ω_n can be determined by the use of the graph when ζ and the lock up time are given.

BANDWIDTH

The -3 dB bandwidth of the PLL is given by

$$\omega_{-3\,dB} = \omega_n \left(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4} \right)^{1/2} \qquad (38)$$

for a type 1 second order[4] system, and by

$$\omega_{-3\,dB} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4} \right)^{1/2} \qquad (39)$$

for a type 2 second order[1] system.

PHASE-LOCKED LOOP DESIGN EXAMPLE

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach

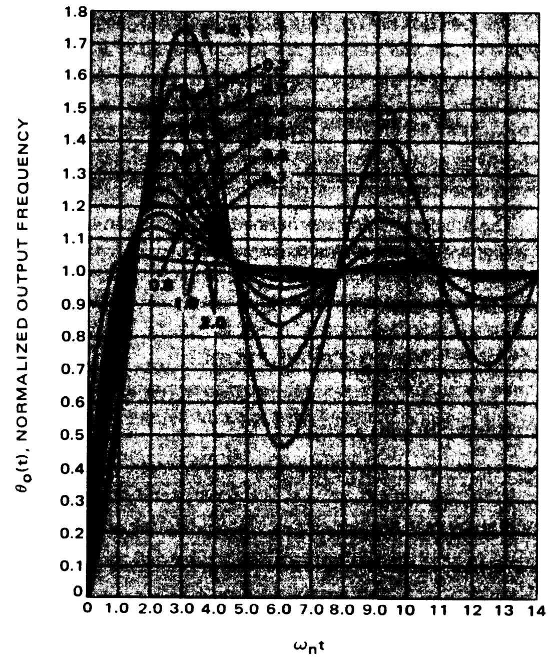


FIGURE 6 – Type 2 Second Order Step Response

to these design constraints is now illustrated. It is desired for the system to have the following specifications:

Output frequency	2.0 MHz to 3.0 MHz
Frequency steps	100 kHz
Phase coherent frequency output	–
Lock-up time between channels	1 ms
Overshoot	< 20%

NOTE: These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer.

From the given specifications the circuit parameters shown in Figure 7 can now be determined.

The devices used to configure the PLL are:

Frequency-Phase Detector	MC4044/4344
Voltage Controlled Multivibrator (VCM)	MC4024/4324
Programmable Counter	MC4016/4316

The forward and feedback transfer functions are given by:

$$G(s) = K_p\,K_f\,K_o \qquad H(s) = K_n \qquad (40)$$

where $\quad K_n = 1/N \qquad (41)$

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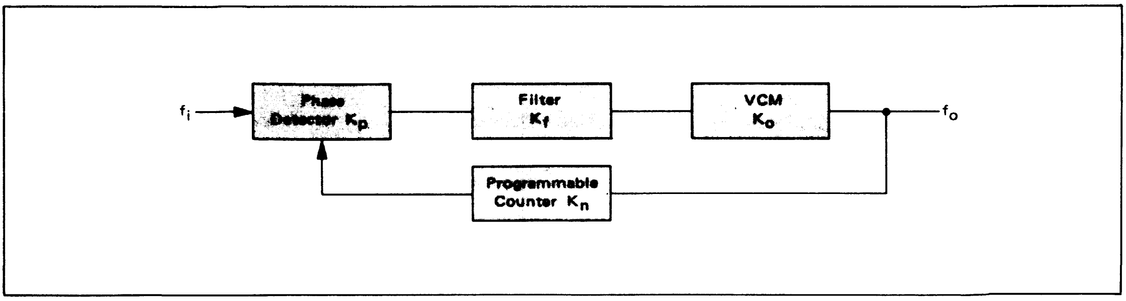

FIGURE 7 – Phase Locked Loop Circuit Parameters

The programmable counter divide ratio K_n can be found from Equation 3.

$$N_{min} = \frac{f_{o\,min}}{f_i} = \frac{f_{o\,min}}{f_{step}} = \frac{2\text{ MHz}}{100\text{ kHz}} = 20 \qquad (42)$$

$$N_{max} = \frac{f_{o\,max}}{f_{step}} = \frac{3\text{ MHz}}{100\text{ kHz}} = 30 \qquad (43)$$

$$K_n = \frac{1}{20} \text{ to } \frac{1}{30} \qquad (44)$$

A type 2 system is required to produce a phase coherent output relative to the input (see Table I). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2 MHz to 3 MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields C = 100 pF. The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

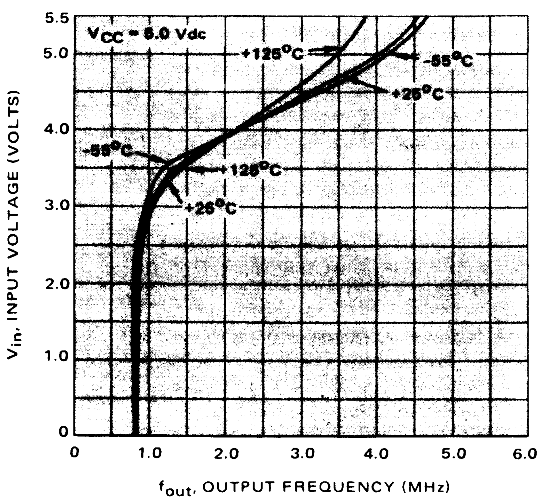

FIGURE 8 – MC4324 Input Voltage versus Output Frequency (100 pF Feedback Capacitor)

The transfer function of the VCM is given by

$$K_o = \frac{K_v}{s} \qquad (45)$$

Where K_v is the sensitivity in radians per second per volt. From the curve in Figure 8, K_v is found by taking the reciprocal of the slope.

$$K_v = \frac{4\text{ MHz} - 1.5\text{ MHz}}{5\text{ V} - 3.6\text{ V}}\, 2\pi \text{ rad/s/V}$$

$$K_v = 11.2 \times 10^6 \text{ rad/s/V} \qquad (46)$$

Thus

$$K_o = \frac{11.2 \times 10^6}{s} \text{ rad/s/V} \qquad (47)$$

The s in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by [5]

$$K_p = \frac{\text{DF High - UF Low}}{2(2\pi)} = \frac{2.3\text{ V} - 0.9\text{ V}}{4\pi} = 0.111 \text{ V/rad} \qquad (48)$$

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 19. The parameters thus far determined include K_p, K_o, K_n leaving only K_f as the variable for design. Writing the loop transfer function and relating it to Equation 19

$$G(s)\,H(s) = \frac{K_p K_v K_n K_f}{s} = \frac{K(s+a)}{s^2} \qquad (49)$$

Thus K_f must take the form

$$K_f = \frac{s+a}{s} \qquad (50)$$

in order to provide all the necessary poles and zeroes for he required G(s) H(s). The circuit shown in Figure 9 yields he desired results.

K_f is expressed by

$$K_f = \frac{R_2Cs + 1}{R_1Cs} \quad \text{for large A} \qquad (51)$$

vhere A is voltage gain of the amplifier.

R_1, R_2, and C are then the variables used to establish he overall loop characteristics.

The MC4044/4344 provides the active circuitry required o configure the filter K_f. An additional low current high 3 buffering device or FET can be used to boost the input mpedance thus minimizing the leakage current from the capacitor C between sample updates. As a result longer sample periods are achievable.

Since the gain of the active filter circuitry in the MC4044/4344 is not infinite, a gain correction factor K_c must be applied to K_f in order to properly characterize the function. K_c is found experimentally to be $K_c = 0.5$.

$$K_{fc} = K_f K_c = 0.5 \left(\frac{R_2Cs + 1}{R_1Cs}\right) \qquad (52)$$

(For large gain, Equation 51 applies.)

The PLL circuit diagram is shown in Figure 10 and its Laplace representation in Figure 11.

The loop transfer function is

$$G(s)\,H(s) = K_p\,K_{fc}\,K_o\,K_n \qquad (53)$$

$$G(s)\,H(s) = K_p\,(0.5)\left(\frac{R_2Cs+1}{R_1Cs}\right)\left(\frac{K_v}{s}\right)\left(\frac{1}{N}\right) \qquad (54)$$

The characteristic equation takes the form

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= s^2 + \frac{0.5\,K_p K_v R_2}{R_1N}\,s + \frac{0.5\,K_p K_v}{R_1CN} \qquad (55)$$

Relating Equation 55 to the standard form given by Equation 34

$$s^2 + \frac{0.5\,K_p\,K_v\,R_2}{R_1N}\,s + \frac{0.5\,K_p\,K_v}{R_1CN}$$

$$= s^2 + 2\,\zeta\,\omega_n s + \omega_n^2 \qquad (56)$$

Equating like coefficients yields

$$\frac{0.5\,K_p\,K_v}{R_1CN} = \omega_n^2 \qquad (57)$$

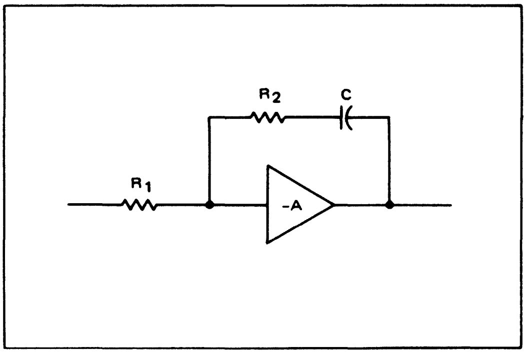

FIGURE 9 – Active Filter Design

and $$\frac{0.5\,K_p\,K_v\,R_2}{R_1N} = 2\,\zeta\,\omega_n \qquad (58)$$

With the use of an active filter whose open loop gain (A) is large ($K_c = 1$), Equations 57 and 58 become

$$\frac{K_p\,K_v}{R_1CN} = \omega_n^2 \qquad (59)$$

$$\frac{K_p\,K_v\,R_2}{R_1N} = 2\,\zeta\,\omega_n \qquad (60)$$

The percent overshoot and settling time are now used to determine ω_n. From Figure 6 it is seen that a damping ratio $\zeta = 0.8$ will produce a peak overshoot less than 20% and will settle to within 5% at $\omega_n t = 4.5$. The required lock-up time is 1 ms.

[redacted]

Rewriting Equation 57

[redacted]

$$= \frac{(0.5)\,(0.111)\,(11.2 \times 10^6)}{(4500)^2\,(30)}$$

$$R_1C = 0.00102$$

(Maximum overshoot occurs at N_{max} which is minimum loop gain)

Let $C = 0.5\ \mu F$

Then $$R_1 = \frac{0.00102}{0.5 \times 10^{-6}} = 2.04\ k\Omega$$

Use $R_1 = 2\ k\Omega$

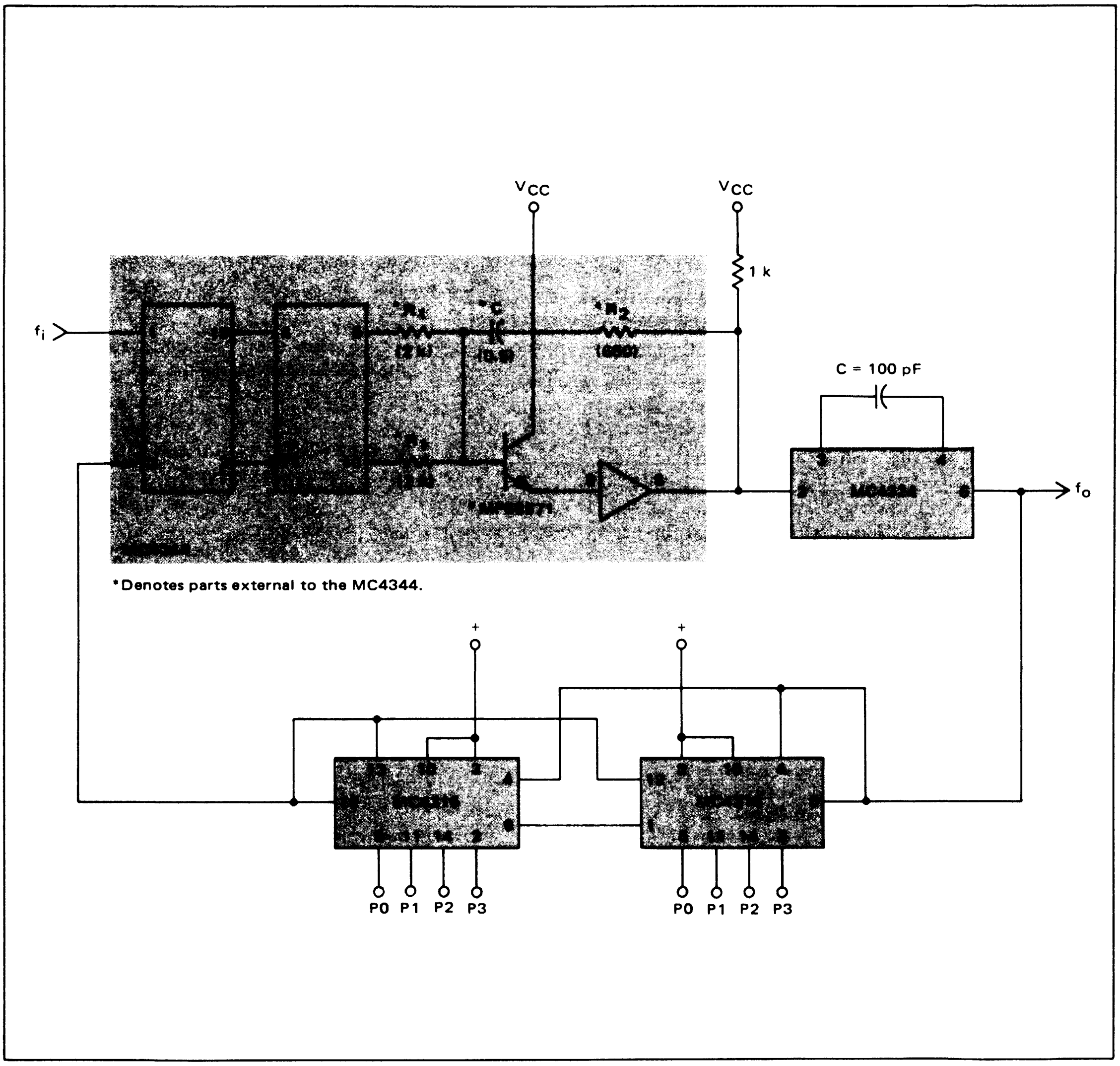

FIGURE 10 — Circuit Diagram of Type 2 Phase Locked Loop

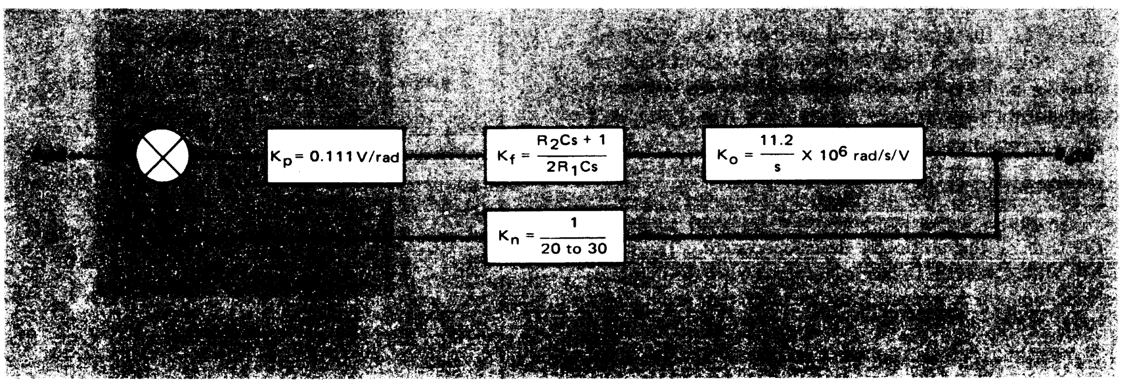

FIGURE 11 — Laplace Representation of Diagram in Figure 10

R_1 is typically selected greater than 1 kΩ.

Solving for R_2 in Equation 58

$$R_2 = \frac{2\zeta \omega_n R_1 N}{K_p K_v (0.5)} = \frac{2\zeta}{C \omega_n} \qquad (63)$$

$$= \frac{2\,(0.8)}{(0.5 \times 10^{-6})\,(4.5\text{ k})}$$

$$= 711\ \Omega$$

use R_2 = 680 Ω

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio K_n, the closed loop poles will vary is position as K_n varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter N = 30. The system response for N = 20 exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

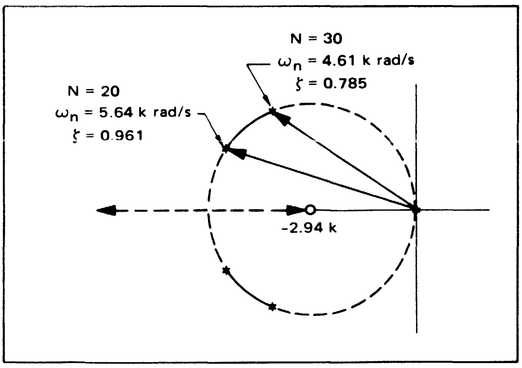

FIGURE 12 — Root Locus Variation

NOTE: The type 2 second order loop was illustrated as a design example because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency a type 2 loop still offers an optimum design.

EXPERIMENTAL RESULTS

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve N = 30 illustrates the frequency response when the programmable counter is stepped from 29 to 30 thus producing a change in the output frequency from 2.9 MHz to 3.0 MHz. An overshoot of 18% is obtained and the output frequency is within 5 kHz of the final value one millisecond after the applied step. The curve N = 20 illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the output frequency is proportional to the VCM control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30 the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrates that the experimental results obtained from the configured system follows the predicted results shown in Figure 13. Linearity is maintained for phase errors less than 2π, i.e. there is no cycle slippage at the phase detector.

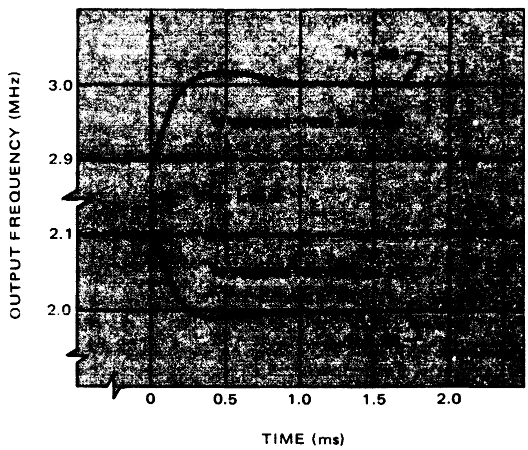

FIGURE 13 — Frequency-Time Response

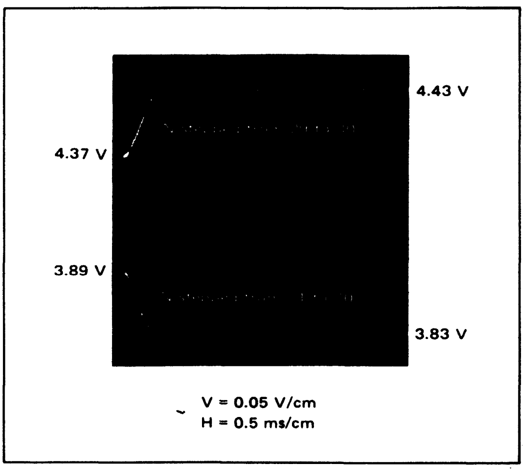

FIGURE 14 — VCM Control Voltage (Frequency) Transient

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*THE PARAMETERS LISTED BELOW APPLY TO THE FOLLOWING PLOT

PHASE DETECTOR GAIN CONSTANT	P1 = 0.111 VOLTS PER RADIAN
VCO GAIN CONSTANT	V1 = 1.12 E+7 RAD PER VOLT
[illegible] RESISTOR	R1 = [illegible] OHMS ($R1_c$ = [illegible])
[illegible] FEEDBACK RESISTOR	R2 = [illegible] OHMS
[illegible] CAPACITOR	C1 = 0.5 MICROFARADS
[illegible] VALUE	N1-N2 = [illegible]
REFERENCE FREQUENCY	F1 = 1[illegible] CPS
OUTPUT FREQUENCY CHANGE	F5 = 1[illegible] CPS

P2 = 0.111	C2 = 0.5
V2 = 1.1[illegible] E+7	N3 - N4 = 21 - 29
R3 = 3[illegible] ($R1_c$ = 2 k)	P2 (F6) = 1[illegible] (1[illegible])
R4 = [illegible]	

PLOT OF FUNCTIONS

(NOTE: Y(T) IS PLOTTED '+', Z(T) IS '*', AND '0' IS COMMON)

FOR T: TOP = 0 BOTTOM = 0.0015 INCREMENT = 0.00005

FOR FCTS: LEFT = 0 RIGHT = 0.12 INCREMENT = 0.002

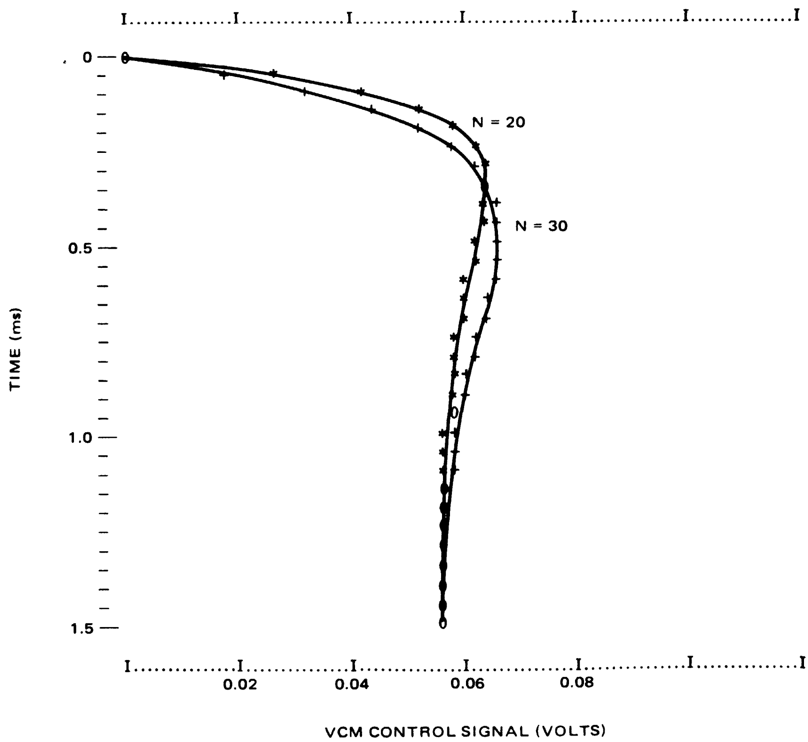

FIGURE 15 — VCM Control Signal Transient

Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 58 and 59 (type 2) as the input variables and is valid for all damping ratios of $\zeta \leq 1.0$. The program prints or plots the control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between the experimental and analytical results.

SUMMARY

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

BIBLIOGRAPHY

1. Topic: Type Two System Analysis
   Gardner, F. M., Phase Lock Techniques, Wiley, New York, Second Edition, 1967
2. Topic: Root Locus Techniques
   Kuo, B. C., Automatic Control Systems, Prentice-Hall, Inc., New Jersey, 1962
3. Topic: Laplace Techniques
   McCollum, P. and Brown, B., Laplace Transform Tables and Theorems, Holt, New York, 1965
4. Topic: Type One System Analysis
   Truxal, J.G., Automatic Feedback Control System Synthesis, McGraw-Hill, New York, 1955
5. Topic: Phase Detector Gain Constant
   DeLaune, Jon, MTTL and MECL Avionics Digital Frequency Synthesizer, AN532

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Typical Applications

Typical Applications 7

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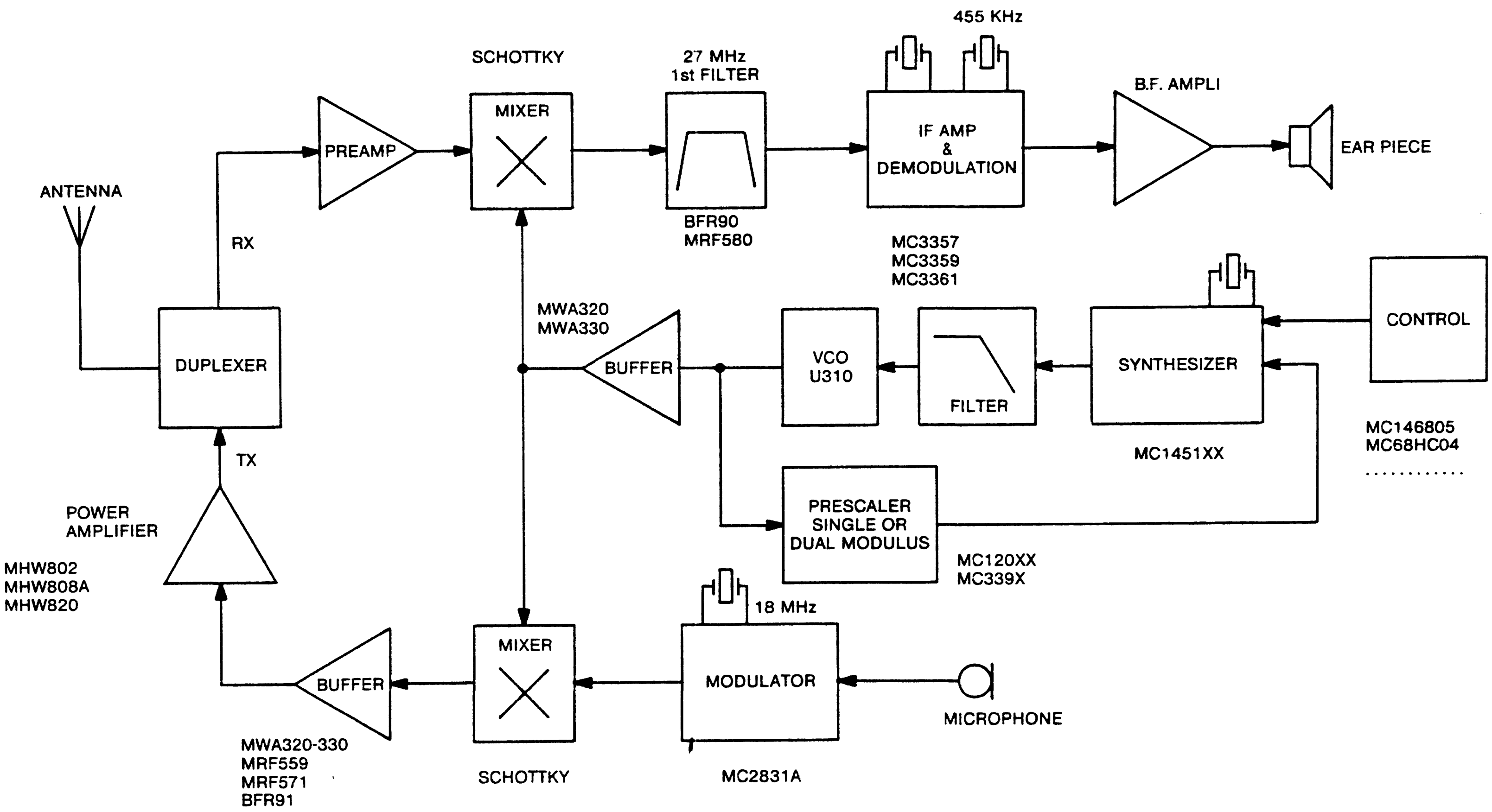
CORDLESS TELEPHONE
USING ONE PHASE LOCKED LOOP



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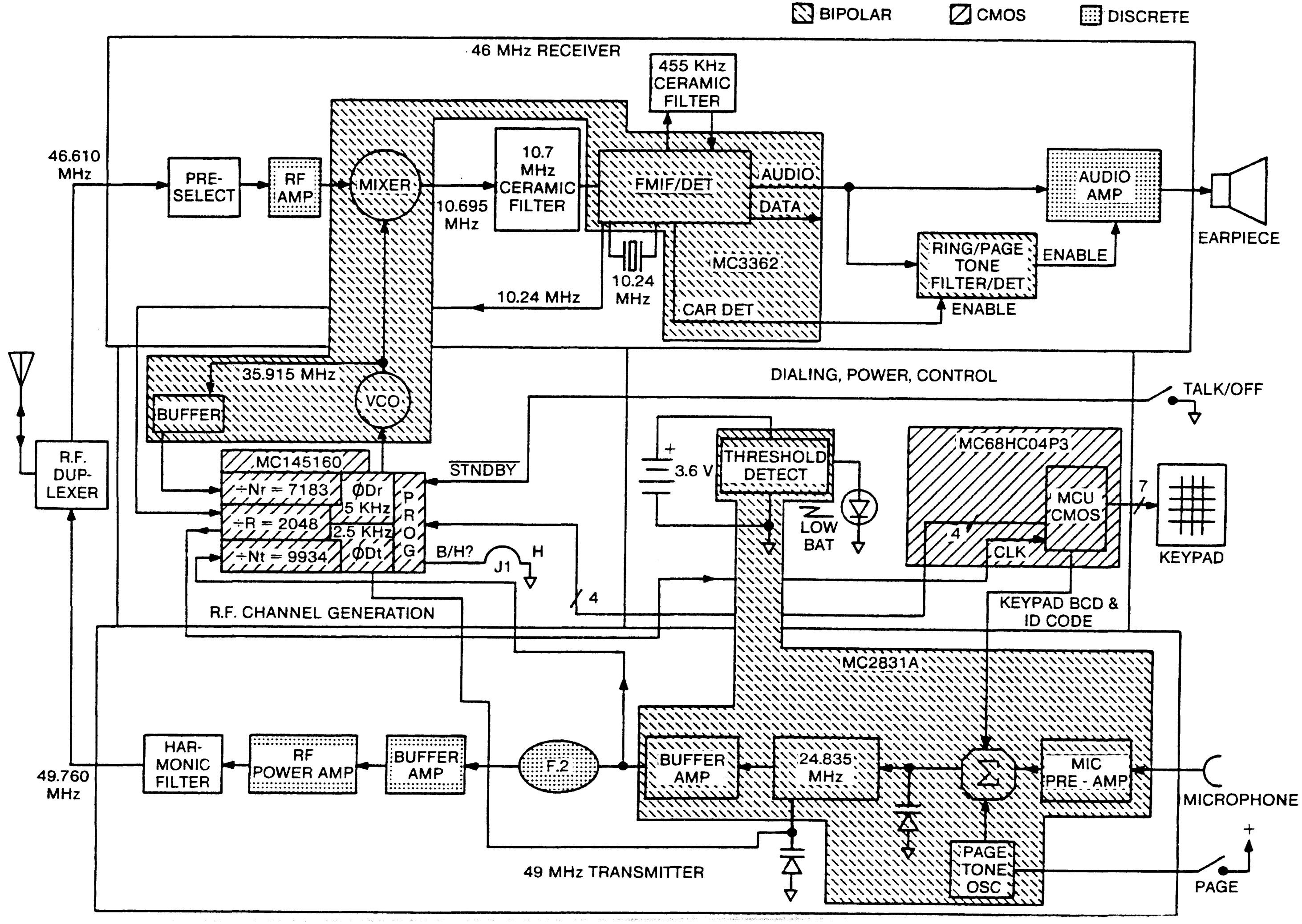
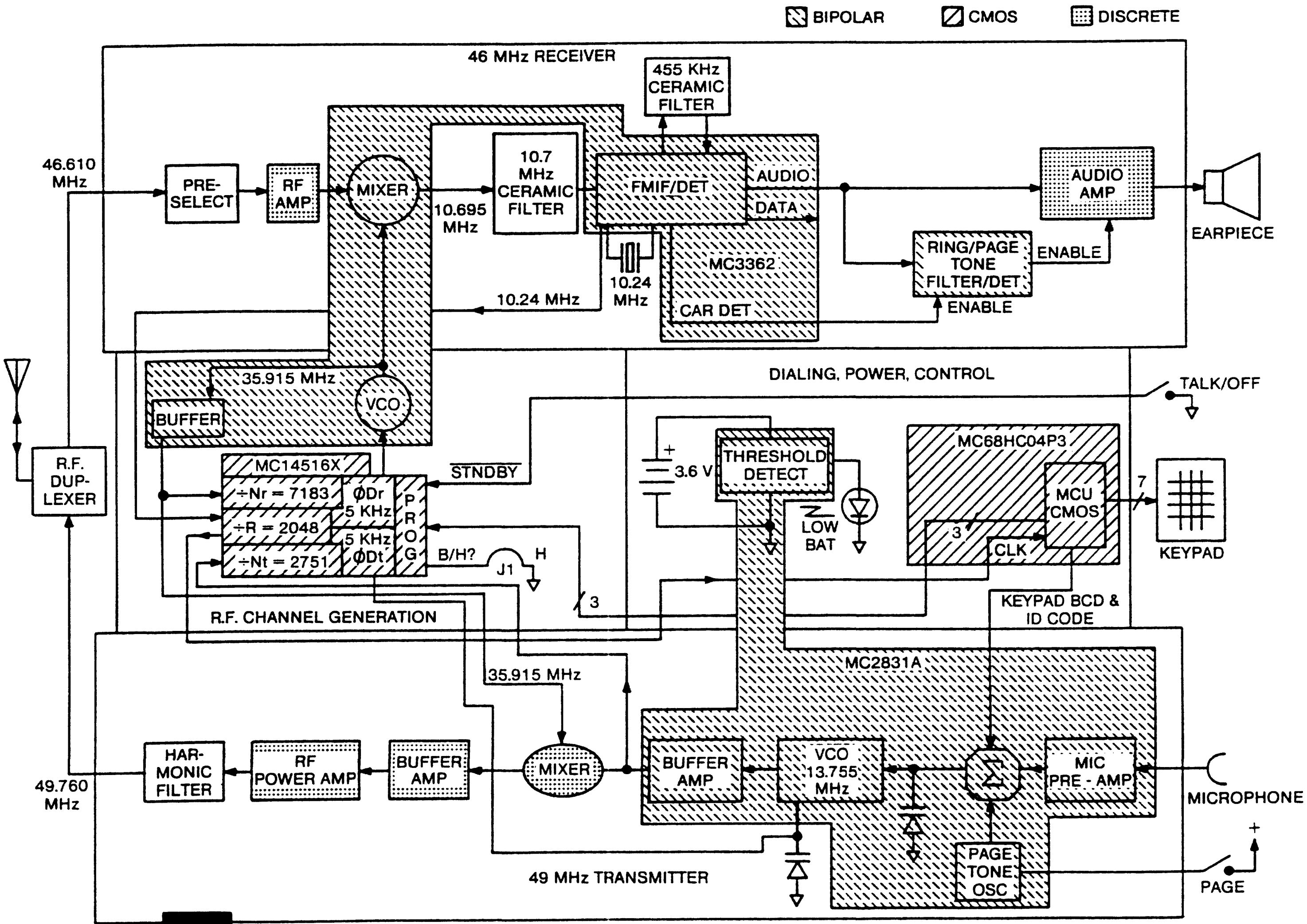
APPLICATION OF DUAL LOOP SYNTHESIZER TO CORDLESS PHONE HANDSET RECEIVER INJECTION AND HALF TRANSMIT FREQ. OSCILLATORS



APPLICATION OF DUAL LOOP SYNTHESIZER TO CORDLESS PHONE HANDSET (RECEIVER INJECTION AND OFFSET OSCILLATORS)



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List of Application Notes
and Engineering Bulletins

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APPLICATION NOTES

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ENGINEERING BULLETINS